International Journal of Research in Engineering, Science and Management
Volume-3, Issue-9, September-2020
journals.resaim.com/ijresm | ISSN (Online): 2581-5792 | RESAIM Publishing

Low Power SAR-ADC Using 180nm CMOS Technology

Shraddha Naik[1*], Bhoomi Patel[2], Chaitali Poojary[3], Sudhakar Mande[4]
[1,2,3]*B.E. Student, Department of Electronics and Telecommunications Engineering, Don Bosco Institute of Technology, Mumbai, India*
[4]*Professor, Department of Electronics and Telecommunications Engineering, Don Bosco Institute of Technology, Mumbai, India*
*Corresponding author: shraddhanaik174@gmail.com

***Abstract*: This paper involves designing of Successive Approximation Register (SAR) Analog-to-Digital converter (ADC) and its implementation in 180nm SCL technology using Ngspice. The paper presents a low power 14-bit, 10Mbps SAR ADC. Low-power design technique has been utilized to achieve the low power consumption that is less than 300mW. ADC is designed in 180nm CMOS technology with a 3.3V power supply and a 10Mbps sampling rate. To achieve low power consumption Charge Scaling DAC, two stage OTA for Sample and Hold and low power D-Flip Flop is used in SAR design.**

***Keywords*: CMOS, Ngspice, OTA, SAR ADC, SCL.**

1. Introduction

A system which processes a signal is a combination of a number of mixed signal circuits, which require both analog and digital domain functions. To change from one domain to other, analog-to-digital (A/D) and digital-to-analog (D/A) converters are used. Analog-to-Digital Converters (ADCs) translate the analog quantities into digital language, used in information processing, computing, data transmission and control systems. ADCs are key components for the design of power limited systems, in order to keep the power consumption as low as possible. Analog to Digital Converters are important building blocks in lots of applications. In past few years, more and more applications are built with very stringent requirements on power consumption. For electronic systems, such as wireless systems or implantable devices, the power consumption is becoming one of the most critical factors. The stringent requirements on the energy consumption increase the need for the development of low voltage and low power circuit techniques and system building blocks. Low power ADCs with moderate resolution and low sampling frequency is suited for biomedical application [1]. These specifications make SAR ADC the suitable choice. It consumes low power due to its simple structure. Moreover, SAR ADC is scalable with the technology scaling since most parts of the architecture apart from the comparator are digital.

2. Successive Approximation ADC

This section describes different components of SAR ADC architecture.

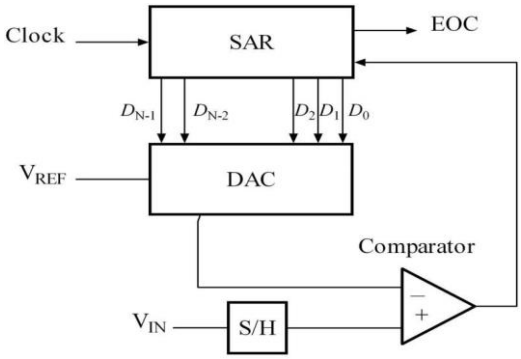

Fig. 1. Functional block diagram

The main components of SAR ADC are a Sample and Hold, a Digital to Analog Converter (DAC), a Comparator and a SAR Logic.

1) A sample and hold circuit to acquire the input voltage.
2) An analog voltage comparator compares input voltage to the output of the internal DAC and outputs the result of the comparison to the SAR.
3) A SAR is designed to supply an approximate digital code of input voltage to the internal DAC.
4) An internal reference DAC that, for comparison with VREF, supplies the comparator with an analog voltage equal to the digital code output of the SAR [2].

3. Design of SAR ADC

To design SAR ADC for given specifications each block needs to satisfy the following requirements:

A. SAR logic

Since expected throughout of ADC is 10Mbps, each flip flop in 14-bit SAR logic must work with minimum clock frequency of 10MHz with on and off time approximately 50ns.

B. Sample and Hold Circuit

To get the required throughput of 10Mbps with 14-bit SAR logic, minimum sample and hold time needs to be less than or equal to 1.4µs. This can be further divided as 0.7µs sample time and 0.7µs as hold time.

C. DAC and Comparator

ADC is expected to work on 3.3V supply with dual rail. This makes 3.3V as dual power supply with 1.65V and -1.65V. With such dual rail power supply resolution of ADC is 100uV. Output of DAC needs to provide resolution of more than or equal to 100uV and comparator must be able to detect this small change and set or reset its output accordingly.

4. Main Components of SAR

A. Comparator

A comparator circuit compares one analog signal with another analog signal, or some reference voltage, VREF and produces an output signal based on its comparison. A comparator generates a logic output high or low based on the comparison between the two analog signals. The comparator is an essential part in the SAR ADC to perform the binary search algorithm. Comparator in the SAR ADC takes more power consumption than the other blocks [2].

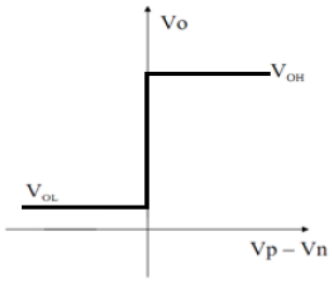

Fig. 2. Voltage transfer characteristics of ideal comparator

Thus a comparator compares two input analog value and gives binary output. In ideal case, binary signals can have two values at any point. But actually there is a transition region between the two binary states. For a comparator, it is important to pass quickly through that transition region.

B. Operational Amplifier

The main building block of analog circuit design is the operational amplifier (op-amp). Its primary use is to provide sufficient gain and to implement all analog signal processing functions using negative feedback.

The open-loop gain of an amplifier is the gain obtained when no overall feedback is used in the circuit. Open loop gain, in some amplifiers, can be exceedingly high. An ideal operational amplifier (op-amp) has infinite open-loop gain. Typically, an op-amp may have a maximal open-loop gain of around 105. The very high open-loop gain of the op-amp allows a wide range of feedback levels to be applied to achieve the desired performance.

In open-loop configuration the input signal is applied to the inverting input terminal of the op-amp and the non-inverting input terminal is connected to the ground. Figure 3 shows the circuit of an open – loop inverting amplifier [3].

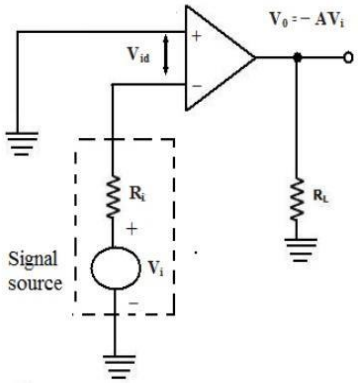

Fig. 3. Open-loop inverting operational amplifier

The output voltage is 180^0 out of phase with respect to the input and hence, the output voltage V is given by,

$$V0 = -AVi$$

Thus, in an inverting amplifier, the input signal is amplified by the open-loop gain A and in phase shifted by 180^0.

C. Sample and Hold

Sample and hold circuit (SHC) contains a switch and capacitor. In the tracking mode, when the sampling signal is high and the switch is connected, it tracks the analog input signal [4].

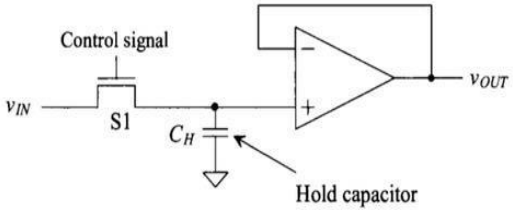

Fig. 4. Sample and Hold Circuit

Then, it holds the value when the sampling signal turns to low in the hold mode. In this case, sample and hold provides a constant voltage at the input of the ADC during conversion. Regardless of the type of S/H, sampling operation has a great impact on the dynamic performance of the ADC. The Sample & Hold uses a capacitor and an analog switch to connect or isolate the capacitor from the input. An operational amplifier connected as follower avoids the effects of the load. The amplifier can be powered down in order to reduce the power consumption when the circuit is in the standby mode.

D. Digital to Analog Convertor

The digital to analog converter (DAC) converts the digital word at the output of the SAR logic to an analog value. Then in

the comparator, this value is compared to the input signal. In this project we are using Charge Scaling DAC as it provides low power dissipation, high speed good accuracy and induces less mismatch errors. It also has fast conversion time. Moreover, they are fabricated easily. The charge scaling DAC works by "binarily dividing the total charge applied to a capacitor array".

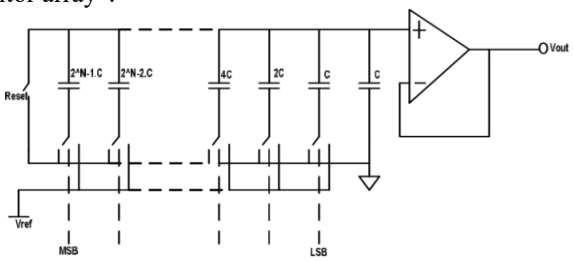

Fig. 5. Charge Scaling DAC

Additionally, the charge scaling DAC has no static power dissipation because when the capacitors have been charged /discharged to their final value no current flows [5].

E. SAR Logic

Successive Approximation Register (SAR) control logic determines each bit successively. Here the SA register contains 14 bit for a 14-bit ADC. There are 3 possibilities for each bit, it can be set to "1", reset to "0" or keeps its value. In the first step, MSB is set to "1" and other bits are reset to "0", the digital word is converted to the analog value through DAC. The analog signal at the output of the DAC is inserted to the input of the comparator and is compared to the sampled input. Based on the comparator result, the SAR controller defines the MSB value. If the input is higher than the output of the DAC, the MSB remains at "1", otherwise it is reset to "0". The rest of bits are determined in the same manner [6]. In the last cycle, the converted digital word is stored. Therefore, a 14-bit SAR ADC takes 14+1clock cycles to perform a conversion. Successive approximation register ADC implements the Binary search algorithm using SAR control logic [2].

5. Experimental Results

A. Comparator

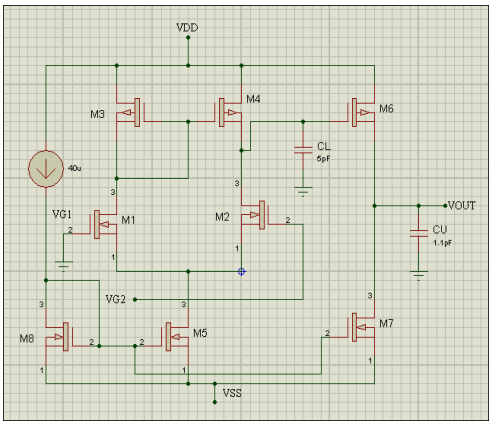

Fig. 6. Design of comparator

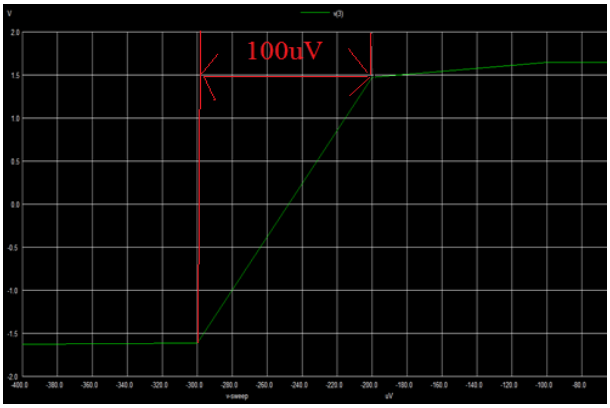

Fig. 7. Transfer characteristics of comparator

The expected resolution of comparator is 100uV and we have obtained the same.

B. Operational Amplifier

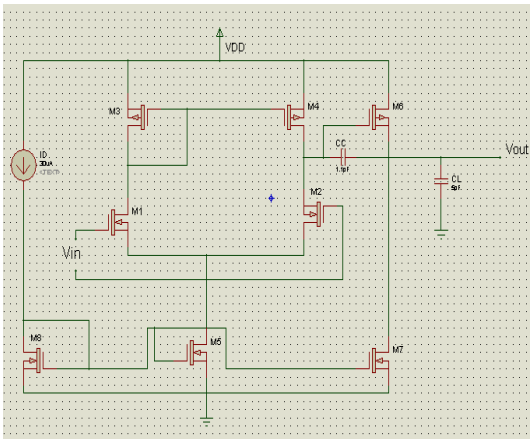

Fig. 8. Design of Op-amp

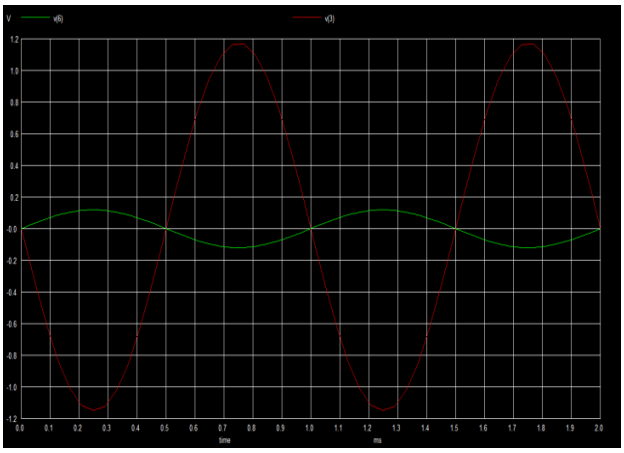

Fig. 9. Waveform of Op-amp

The expected gain of Op-Amp should be more than 5000 and we have obtained 5800.

C. *Sample and Hold Circuit*

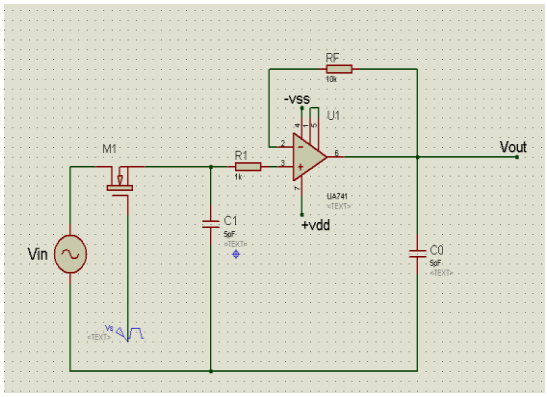

Fig. 10. Design of Sample and Hold Circuit

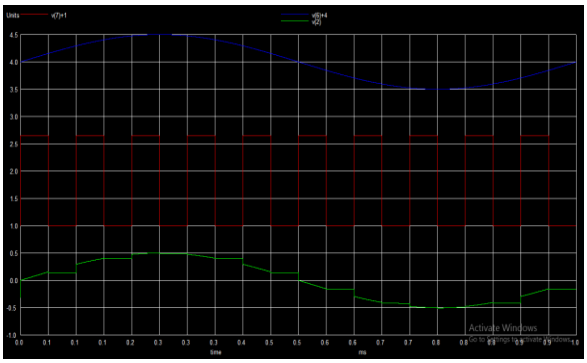

Fig. 11. Waveform of Sample and Hold Circuit

The expected hold time is 0.7µs and the obtained hold time is 50µs. The expected sample time is 0.7µs and the obtained sample time is 50µs.

D. *Digital to Analog Converter*

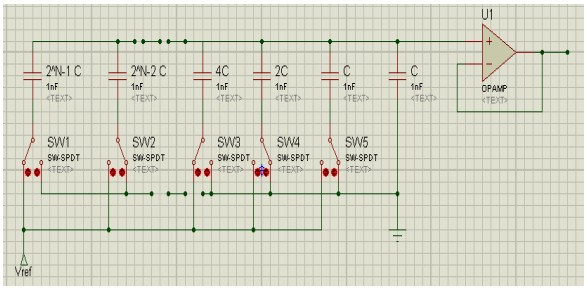

Fig. 12. Design of DAC

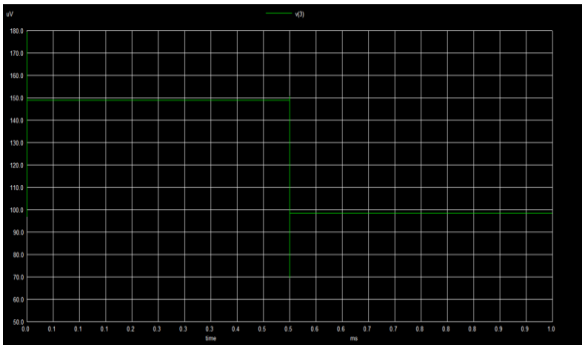

Fig. 13. Waveform of DAC

The expected resolution should be greater than that of comparator and we have obtained 100.7µV.

E. *D'Latch*

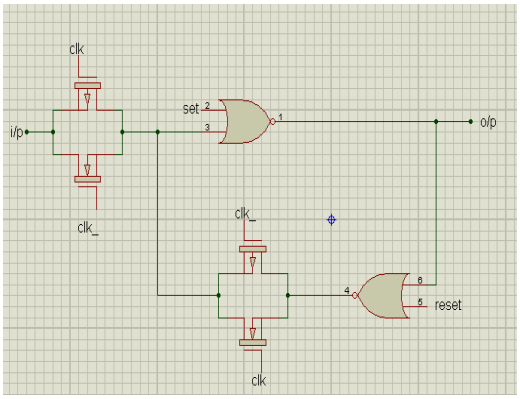

Fig. 14. Design of D'Latch

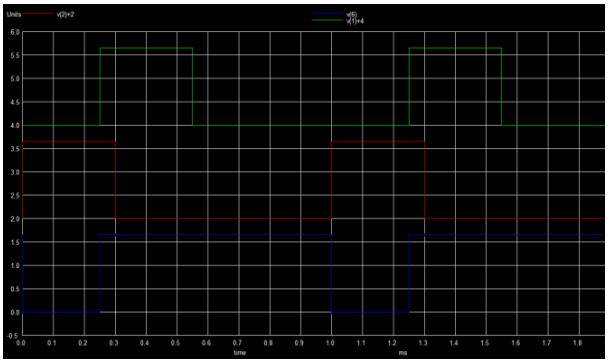

Fig. 15. Waveform of D'latch

Here we plotted the graph of D'Latch. It works without set and reset at 0.1µs. So we have to add set and reset signal for better performance.

6. Results

Power Consumption of each block is shown in the table 1 below,

Table 1
Power Consumption of each block

Block	Power Consumption
SAR	13.197mW
DAC	241.5uW
Comparator	231uW
Op-Amp	241.5uW
Sample and Hold	241.5uW
Total	13.435mW

7. Conclusion

In this paper, low power and high speed SAR ADC is proposed and designed in 180 nm CMOS technology. We presented high speed/performance and typically low power consumption design of Successive Approximation Logic for ADC and by using the same we designed ADC architecture for SAR to work efficiently the time period calculated is 1.4µs.

Therefore, its frequency of operation is 1/1.4µs=714. 28kHz.The gain of Op-Amp is 5800.The resolution obtained for the comparator is 100µV and for the DAC is 100.7µV. Since the resolution of DAC is more than comparator the conversion of DAC value will be done easily without any delay. The expected hold time for sample and hold circuit according to our specifications should be 0.7µs but the hold time we have obtained is 50µs. The sampling frequency obtained is 22.14 KHz. The flip flop in SAR works at 0.1µs for 1 clock cycle. Finally, we club up all the working modules of the SAR based ADC is designed in 180nm CMOS technology.

References

[1] Jitendra A. Waghmare, P. M. Ghutke, "Design of Low Power Successive Approximation Analog to Digital Converter," May 2014.
[2] Md. Kareemoddin, A. Ashok Kumar, and Syed Musthak Ahmed, "Design of Low Power Comparator for SAR ADC in Biomedical Applications," July 2013.
[3] T. Sowmya, SK. Muneer Nihal, and D. Gopi Chand. "Implementation of 16-bit pipelined ADC using 180nm CMOS technology," March 2018.
[4] R. J. Baker, "CMOS Circuit Design, Layout, and Simulation," 3rd Edition; Wiley-IEEE; 1208 pages; 2010; ISBN 978-0-470-88132-3.
[5] Priyanka T, H. S. Aravind, Yatheesh H. G, "Design and implementation of two stage operational amplifier," International Research Journal of Engineering and Technology, vol. 4, no. 7, July 2017.
[6] Lalit Madhab Dhal, and Anshuman Pradhan, "Study and analysis of different types of comparators", 2013.