International Journal of Research in Engineering, Science and Management
Volume 6, Issue 3, March 2023
https://www.ijresm.com | ISSN (Online): 2581-5792

An Instinctive Error Encoder and Decoder Using XOR for Space Applications

Shanigaram Dilip[1*], Varaganti Priyanka[2]
[1,2]Department of Electronics and Communication Engineering, Jawaharlal Nehru Technological University, Hyderabad, India

***Abstract*: Memory errors are a significant concern in advanced electronic circuits. As technology advances, on-chip memories become more susceptible to multiple bit errors. To address this issue, error detection and correction techniques (ECC) are used to identify and rectify corrupted data during transmission. In this study, a multiple bit error detection and correction method is proposed to reduce the impact of radiation-induced MCUs in memory for space applications. An inversion methodology is used to implement the encoding process, which involves analyzing diagonal bits, parity bits, and check bits through XOR operations. To recover data, an XOR operation is performed between the encoded bits and the recalculated encoded bits. This is followed by an analysis, verification, selection, and correction process. Compared to existing methods, this approach is more power-efficient and requires minimal space and delay. The proposed ECC scheme is designed to mitigate data corruption in volatile memories and is simulated and synthesized using Xilinx in Verilog HDL. This design approach provides high performance, low path delay, and improves synchronization.**

***Keywords*: ECC (Error detection and correction Technique), Multiple cell upsets, XOR gates, Verilog HDL.**

1. Introduction

This study focuses on the issue of soft errors in electronic circuits, particularly in memories, in space due to high temperatures. One way to reduce these errors is by maximizing critical charge or using error correction codes (ECC), but single error correction (SEC) is not effective for multiple cell upsets (MCUs) where two or more bits in the same memory are affected. Interleaving methods have been proposed, but they increase system complexity and impact area and power consumption. A new ECC method is proposed by Zhu et al. to reduce radiation-exposed multiple bit upsets in memories by detecting and correcting adjacent double bit errors and reducing non-adjacent double bit errors. It reduces hardware redundancy by 40% and is more efficient than existing ECC codes. Pedro et al. introduced an efficient single and double adjacent error correcting parallel decoder for the (24, 12) extended Go lay code. The decoder uses a 12-bit OR gate for the implementation of foremost and the rest is implemented using a 24-bit OR gate.

2. Existing Solution

A new error correction 2-dimensional code (2D-ECC) is proposed. This algorithm detects and corrects errors effectively when relates with other existing error correction techniques. This performs data region division, redundancy and syndrome calculation, verification and region selection one by one to recover the original data. Boolean XOR operation is performed which is most widely used in cryptography and also in generating parity bits for error checking and fault tolerance. This 2-dimensional algorithm performs encoding-decoding process which codifies 16-bit input data into 32 bits in encoding and while decoding again the original 16-bit data is recovered.

Process of encoding:

First, divide the 16 input bits into four groups (Xi, Yi, Zi, Wi). The diagonal bits (Di), parity bits (Pi) and check bits (Ci) are determined using XOR operation. In the process of encoding, the input 16 bits gets converted into 32 bits (redundancy bits).

Process of decoding:

In decoding, the syndrome calculation has been analyzed with the encoded data and the recalculated encoded bits (SDi, SPi and SCi). After that, verification, region selection and correction can be performed.

Existing Algorithm:

STEP 1: Read the input 16-bit data (A16 – A0)

STEP 2: Divide the input data into 4 groups

X_1	Y_1	Z_1	W_1
X_2	Y_2	Z_2	W_2
X_3	Y_3	Z_3	W_3
X_4	Y_4	Z_4	W_4

STEP 3: Analyze diagonal bits, parity bits and check bits using XOR operation.

Diagonal bits (D1, D2, D3, D4) using XOR operations the 2×2 matrix,

$$D1 = X1 \oplus Y2 \oplus Z1 \oplus W2$$
$$D2 = X2 \oplus Y1 \oplus Z2 \oplus W1$$

Parity bits (P1,P2,P3,P4) using XOR for operation taking the

*Corresponding author: shanigramdilip@gmail.com

first bits, second bits, third bits and the fourth bits from the groups.

$$P1 = X1 \oplus Y1 \oplus Z1 \oplus W1$$
$$P2 = X2 \oplus Y2 \oplus Z2 \oplus W2$$

Check bits (Cx, Cy, Cz, Cw) using XOR operation by taking the alternative bits.

$$Cx13 = X1 \oplus X3$$
$$Cx24 = X2 \oplus X4$$
$$Cy13 = Y1 \oplus Y3$$
$$Cy24 = Y2 \oplus Y4$$

STEP 4: Calculate the syndrome values for diagonal, parity and check bits by performing XOR operation between the redundancy data stored and the recalculated redundancy bits (RDi, RPi, RCi).

$$SDi = Di \oplus RDi$$
$$SPi = Pi \oplus RPi$$
$$SCi = Ci \oplus RCi$$

STEP 5: Check the following conditions to identify the error that to be satisfied.

- SDi and SPi bits have atleast one value similar to 1
- More than one SCi value was similar to 1

STEP 6: Perform region selection and change the erroneous data to get the corrected output.

3. Proposed Solution

A typical system-level technique to harden memory against multiple bit upsets (MBUs) would be the use of error correction codes (ECCs) for enhanced correction capabilities. Building updated ECCs with low redundancy and correction of errors however has been a significant issue, especially about adjacent ECCs. Present MBU mitigation codes concentrate primarily on correcting up to 3-bit explosive errors. The amount of impaired bits will quickly extend to even more than 3 bit as that of the software scales as well as the cell interval gap decrease. In this article, a technique for 4-bit bursting bug fix (BEC) codes was introduced with a Multiple bit error detection and correction (MBEDC) codes.

4. Implementation

The implementation of the project design can be Software implementations.

Software Requirements

- Xilinx ISE 14.5

Although several Error Correction Codes (ECCs) are capable of detecting and correcting a certain number of errors, their use is limited due to the complexity of decoding methods and constraints on key length. In most cases, these codes can only fix errors in adjacent bits, making them insufficient for other error patterns. Therefore, memory radiation susceptibility has become a major concern in maintaining the safety of electronic devices. Two common consequences of radiation-induced failures in contemporary static random-access memories (SRAM) are single event upset (SEU) and multi-bit upset (MBU).

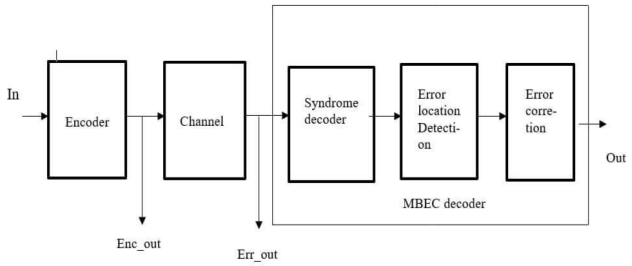

Fig. 1. Proposed block diagram

In memory-hard designs, ECCs that correct adjacent bits are common, with many codes suggested, including double adjacent error correction (DAEC), Triple Adjacent error correction (TAEC), and 3-bit Burst (BEC) error correction. SEC or SEC-DED code paired with interlocking of memory cells is also an alternative to codes that can fix any adjacent errors. The article suggests that 3-bit BEC codes have been strengthened to include Multiple bit error correction (MBEDC) codes.

In Verilog hardware definition language (HDL), the encoders and decoders for MBEDC codes are introduced. The region and latency overhead were moderate to improve the correction capacity compared to the previous 3-bit BEC codes.

Binary Block Linear Codes:

During the receiving code, errors can occur and these errors can be represented by the velocity error e (e0, e1, ... ,en-1), which signals the presence of an error throughout the ith bit, ei=1. If a codeword r with the Error Vector e = (e0, e1, ... ,en-001) has several bit mistakes, the code syndrome can be determined by using the formula in respect of the error vector. S = e · HT (5). OLS codes are built on the foundation of Latin Squares. OLS codes are a product of OLS protocols and have k = m2 and 2tm known as descriptive, where t is the error number which can be corrected. The code t = 2 and thus 4m search bits can be used for double error checking. The decoding process begins with the singular value bits being recalculated and the retained parity check bits verified. OLS codes are developed from the parity search matrix H, and the structure of the matrix is used to repair further mistakes. In summary, the encoder uses the G matrix.

Procedure of Encoding and Decoding for MBEDC Codes:

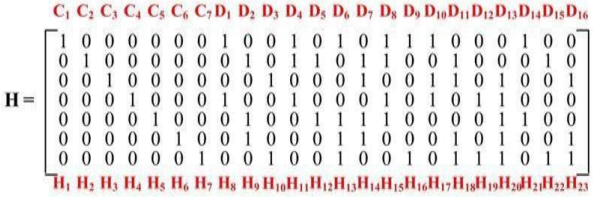

Fig. 2. Parity check matrix

Data Input:
Data [D1:D16] = 1 1 0 1 1 1 0 0 1 1 0 0 1 1 1 1

Encoding Process:

Bits Flipped:

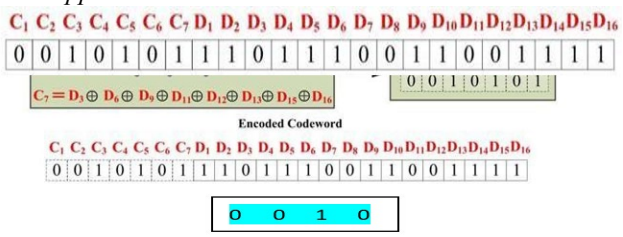

Fig. 3. Code word stored in memory

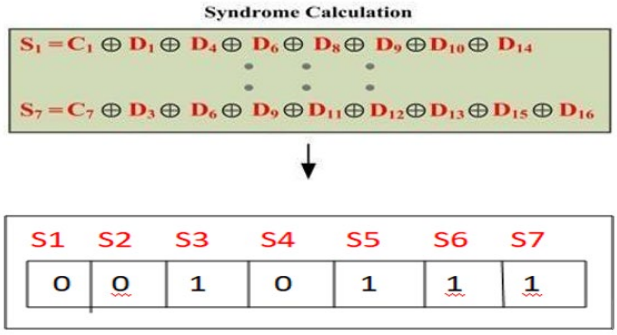

Fig. 4. Decoding process

Data output:
1 1 0 1 1 1 0 0 1 1 0 0 1 1 1 1

That H matrix used throughout Fig is seen in an illustration for 16 transmitted data below. 3.1. The Commission's plan. That check bits were determined either by corresponding transmitted data depending on the structure of the parity check matrix. That latest codeword, verify bits even data bits are saved throughout the memory. That material of damaged memory cells is changed as the particles enter the memory that contributes to MBUs.

5. Conclusion

To summarize, the project introduces a novel error correction code (ECC) that is designed to mitigate data corruption in volatile memories. The proposed ECC employs multiple bit error encoding and decoding, and has been simulated and synthesized using Xilinx implemented in Verilog HDL. This approach yields high performance and low path delay. While also reducing synchronization issues through the use of an inversion operation method. Additionally, the proposed scheme is particularly notable for its ability to handle large word sizes, such as those found in caching, where OLS codes are currently being utilized.

References

[1] R. C. Baumann, "Soft errors in advanced computer systems," IEEE Des. Test. Comput., vol. 22, no. 3, pp. 258-266, 2005.

[2] E. Ibe, S. Chung, S. Wen, H. Yamaguchi, Y. Yahagi, H. Kameyama, S. Yamamoto and T. Akioka, "Spreading diversity in multi-cell neutron-induced upsets with device scaling," in Proc. IEEE Custom Integrated Circuit Conf., pp. 437-444, 2006.

[3] P. Reviriego, J. A. Maestro and C. Cervantes, "Reliability analysis of memories suffering multiple bit upsets," IEEE Trans. Device Mater. Rel., vol. 7, no. 4, pp. 592- 601,2007.

[4] P. Reviriego, J. Maestro, S. Wen and R. Wong, "Protection of memories suffering MCUs through the selection of the optimal interleaving distance," IEEE Trans. On nuclear science., vol. 57, no. 4, pp. 2124-2128, 2010.

[5] P. Reviriego, J.A. Maestro, Luis-J. Saiz-Adalid and S. Pontarelli, "MCU tolerance in SRAMs through low-redundancy triple adjacent error corrrection," IEEE Trans. On very large scale integration (VLSI) systems., pp. 1-5, 2014.

[6] P. Reviriego, S. Liu, L. Xiao and J. Maestro, "An efficient single and double adjacent error correcting parallel decoder for the (24, 12) extended golay code," IEEE Trans. On very large scale integration (VLSI) systems, pp. 1-4, 2015.

[7] N. Aragon, P. Gaborit, A. hauteville, O. Rautta and G. Zemor, "Low rank parity check codes: New decoding algorithms and applications to cryptography," IEEE Trans. on information theory., pp. 1-21, 2017.

[8] D. Digdharsini, D. Mishra, S. Mehta and TVS Ram, "FPGA implementation of FEC Encoder with BCH and LPDC codes for DVB S2 system," Inter. Conf. on Signal processing and Integrated Networks, pp. 78-81, 2019.