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Energy Efficient Power Gated True Single Phase Clocked Flip Flop with Redundant Precharge Free Operation

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***Abstract*: The project represents the analysis of a novel energy gated true single phased clock (TSPC) flip flop. Optimizing the power is a major aspect in many applications. The concept of the project attributes to present D flip-flop circuit using header power gating technique which is significantly used for low power operation. The task of the analysis is to verify the energy loss of the data flip flop in the suspected functional design. This proposed design is implemented in Tanner EDA tool. The evaluation and simulation output shows a huge decrease in energy consumption for this proposed cell with power gating.**

***Keywords*: Header power, TSPC flip flop, optimization, novel energy.**

1. Introduction

While designing integrated circuit the major issue is the power consumption. The performance and the reliability is affected by the large heat dissipation. By increasing the battery life power dissipation can be reduced. Flip flop play role in many digital circuits. Decreasing the energy dissipation in data flip flops results in limiting consumption of power. The rapid growth in Internet of Things (IOT) platform in different application like health care, transportation and smart eco-systems leads to the deployment of the IOT devices, means that the processors are becoming wide spread. However, due to the extinct widespread of digital devices creates an idea to reduce the work and power utilization and its demands, which can also be achieved by using the smaller batteries which reduces the cost and size. Flip flop is directed by input to change the state. Here we discuss about data FF, this flop is a best priority flop widely applied in auto electronics. This flip flop is used in counters, shift registers.

The excessive heat generated while testing the very large-scale integration (VLSI) circuits leads to destroy chip which is used for testing. By adopting SCAN test method, more executable complementary metal oxide semiconductor (CMOS) circuits utilize available dynamic power during testing because of its enhanced switching performance. The power and energy consumption of digital systems may increase notably during testing. But the reliability of circuit may reduce due to the more power consumption. The switching performance created in the circuit during testing application may directly corresponds to the power or energy consumption. This results in diminishing the battery life during various testing. A scanned based testing method includes to apply patterns of test from a scan chain load to a circuit under test (CUT).

The thermal and electrical limit of the system requirement and the limit of the components are determined by the average power consumption. If these limits exceed there may be deviation in the circuit functionality from the actual working. The main idea of having power into consideration in testing field is the power/ energy of a digital circuits is higher in test mode than in system mode, because the test patterns for many combinational circuit nodes can switch only when a system mode power saving is activated for a few modules at same time. Also, the functional input vectors applied to a given circuit in the successive pattern during system mode have a major correlation. There is no specified relation between the consecutive test patterns generated by an automatic test pattern generation (ATPG) tool or by a linear feedback shift register (LFSR) i.e., for built in self-test (BIST) for testing such circuits. This creates a large switching task in the given circuit under test operation than in the normal operation. Since power dissipation in complementary metal oxide semiconductor (CMOS) circuits is directly dependent on switching task, this switching analogy results during test can create many difficulties thereby increases power in the circuit and responsible for increased cost, reduced reliability, variation in the test operation and other technical problems. Hence reducing the energy/power dissipation in testing area has become a very important criteria in VLSI schematic, also a major objective in the coming future.

The hard errors observed by permanent physical damage which cannot be recovered in digital field, soft errors are caused by radiation or voltage/current variations that lead to transient changes in the internal node, thus they are temporary errors. Thus, due to the unknown occurrence of soft errors, it is desirable to develop soft error tolerant designs. Therefore, soft error tolerant design techniques have been created a great research interest.

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2. Objectives

a) Effective reduction in power utilization and power delay product.
b) The path of short circuit can be avoided using the analysis of floating node.
c) The area can be decreased by removing the unused transistors.
d) By adopting clock working at low frequency, flip-flops are made to work correctly.
e) More than 80% power consumption can be saved.

3. Methodology

Power electronics are increasing their productivity in an enormous way. Some of the electronics systems in the growing environment are micro phones, microelectronic circuits etc. Complexity of the system is getting reduce in a daily usage of electronic application, researcher may fail in reaching the expectation of the benefit of providing low powered dissipation equipment's. The power dissipation utilizes thirty five percent of the energy at nanometer level. Main goal for the proposed study is analyzing the feature of the most acceptable way to design a chip using low power which is known as "Power Gating". The main interest of the study is on CMOS devices in nanometer scale, as this technology is most widely accepted method in present physical design systems. In the "power gating" technique, a circuit can operate in two different modes, i.e., ACTIVE mode and SLEEP mode.

The sleep switches are turned high and can be viewed as the functional inefficient resistances in active mode. The sleep switches are turned low to reduce the leakage power in sleep mode. A sleep switches is at the VDD then it is called as "Header switch". A sleep switches is at ground then it is called as "Footer switch". Here for the proposed method, we use header power gating technique. For modern design, to implement very large-scale integration circuit, power has become a major criterion to be noticed. By scaling down to sixty-five nanometer the leakage power can become an important component of the overall power dissipation in the complementary metal oxide semiconductor (CMOS) circuits [1]. Sleep transistor (ST) are used as switches to off the voltages of the circuits. A sleep transistor is termed either as P-type MOS or N-type MOS high threshold voltage, V_{th} transistor that connects potentials to circuit and it is named as "virtual power supply". The P-type MOS sleep transistor is used to activate VDD supply and is named as "header switch". The N-type MOS sleep transistors Controls ground and is named as "footer switch". This is implemented using 90nm designs, hence either header or footer switch is considered.

Power gating technique is one of the important concepts to design and implement sleep transistor. The schematic of power gated flip flop is shown in fig. 1. The few standards taken into consideration for the sleep transistor to design are length of the gate, width of the gate, area, leakage current and efficiency. In the "power gating" method, sleep transistors are used as switches to off the power to various elements of a design in standby mode. VDD supply is controlled by P-type MOS header switch implementation. P-type MOS transistor is having leakage current than N-type MOS transistor of the same size. The drawback of the header switch is that PMOS has low drive current than NMOS of a same size. As a result, a header switch implementation usually consumes more area than a footer switch implementation. The footer switch is implemented by NMOS transistor to control VSS supply.

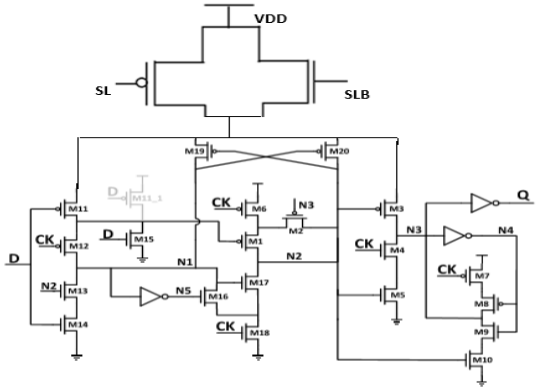

Fig. 1. Schematic of Power Gated Flip Flop

By adopting scaling process frequently there will be an enormous increase in chip production and enlarges density and allows more elements in a small area which implies that there is a consumption of energy. In real time applications number of cells in an electronic appliance is having a wide advantage to make us of battery in an efficient manner. Examples are mobile phones, house hold appliances and personal computers. Also, in servers and advanced computing machines, power consumption results in heat dissipation resulting in expensive cooling techniques. Hence it is important to slow down the low power machines to serve the above requirement.

Dynamic power usage and fixed power usage are two categories of digital circuits [3] and [5]. Dynamic power dissipation is caused by the charging and discharging of the transistor capacitance and wire capacitance. Scaling acquires decreasing potential to avoid the disturbance of transistors because of the high induced electric field. Voltage scaling retains valuable mass of dynamic power. Threshold potential scaled to increase the performance [6]. But there is a raise in leakage. Threshold potential and leakage results in an exponential dependency. Therefore, leakage power is termed as static power and is a large fraction of the overall power consumption.

Leakage power was observed and recorded to be forty percent of the overall power consumption of 130 nanometer complementary metal oxide semiconductor methodology. "Power gating" is the one of the important and efficient paths to get less power result. When the circuit is standby mode, the circuit power is removed by including one transistor which controls the other transistors to modify the changes as per the design requirement and is called as sleep transistor [4]. As the power is directly depends on the square of the potential, "Power gating" circuit decreases an efficient amount of leakage power [7]. Later, the HIGH threshold voltage transistors as sleep

transistors and LOW threshold voltage transistors as logic analysis gives the total power savings which manages the circuit performance [8]. The main aim here is to save maximum power by allowing the circuit to be in ON condition as long as the required data is sent to perform the functionality, and switches OFF the power automatically when the circuit finishes the work. The goal is to save power without loss of efficiency and speed.

In this project, a power gated true single phase clocked (TSPC) flip flop is used to minimize the power dissipation. This involves two transistors of PMOS and NMOS running in parallel such that header power gate works in active mode when required and acts as sleep mode when it is disconnected, thereby power utilization is achieved.

4. Implementation

In this project the solution for the testability of design of any integrated circuits are implemented using tanner EDA tool. It is a software solution for the design, verification and validation of the signal. Tanner EDA focuses on the following area:

a) Allows to input schematics of the circuit
b) SPICE simulation performance
c) The elements are physically designed
d) Allows to performs design rule check (DRC) testability
e) Checks for layout versus schematic (LVS) testability

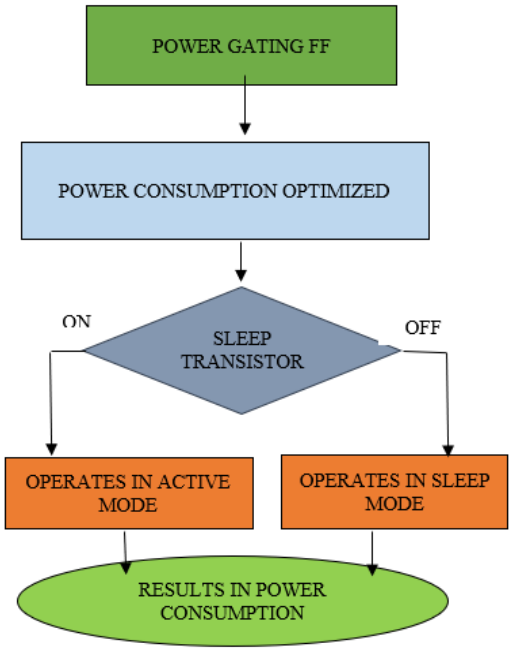

Fig. 2. Flow chart of the proposed method

The above flow chart depicts the proposed method. In this the suggested flip flop, the operation performed only when the sleep transistors are in progress which is also termed as active mode of operation. The supply to the circuit is disconnected by shutting down the transistors. Since supply is disconnected, the power dissipation of circuit is minimized in this mode and it is termed as sleep mode. The header power gating technique is employed in our proposed method.

5. Results

The circuit analysis of the power gated flip-flop is illustrated in fig. 3. It is designed to minimize the power dissipation.

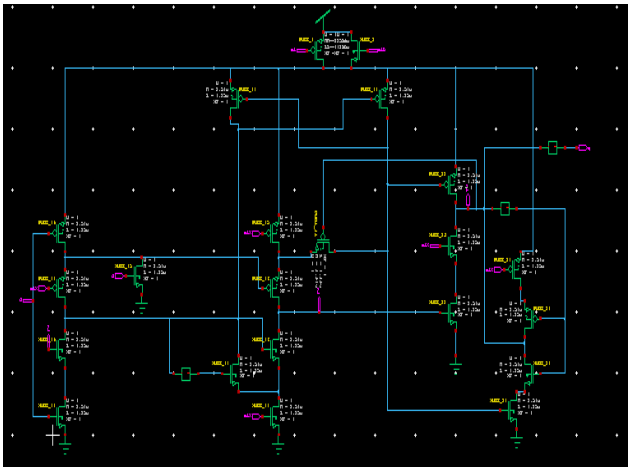

Fig. 3. Schematic of Proposed Flip Flop in S-Edit

The proposed method consists of PMOS and NMOS transistor running in parallel. Both the transistor inputs are in inversion, sl is the input to PMOS and slb is the input to NMOS, by disrupting the path between supply and ground power consumption can be achieved. When supply is connected, the transistors are active and it is termed as Active mode. Since supply is disconnected, the power dissipation of circuit is minimized in this mode and it is termed as sleep mode

The output for Area is as shown below for the proposed project.

```
Device and node counts:
          MOSFETs - 26
             BJTs - 0
          MESFETs - 0
        Capacitors - 0
         Inductors - 0
Transmission lines - 0
   Voltage sources - 3
             VCVS - 0
             CCVS - 0
V-control switch - 0
    Macro devices - 0
      HDL devices - 0
       Subcircuits - 0
Independent nodes - 117
      Total nodes - 121
```

Fig. 4. Proposed` Flip Flop – Area

Here Device and node counts: MOSFETs - 26 represents Area. About 45% of area is utilized in proposed method. The output of area consumed by the proposed power gated TSPC FF is as illustrated in fig. 4.

The output for power is as shown below for the proposed project.

The power consumption of the proposed method achieved is about 42%. The output of power consumed by the proposed power gated TSPC flip flop is as shown in fig. 5.

```
* BEGIN NON-GRAPHICAL DATA

Power Results
v5 from time 0 to 1e-007
Average power consumed -> 2.090793e-004 watts
Max power 5.455454e-004 at time 1.16065e-008
Min power 7.871567e-005 at time 1.01879e-008


* END NON-GRAPHICAL DATA
```

Fig. 5. Proposed Flip Flop- Power

The output for Ares is as shown below for the proposed project.

```
* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

delay = 7.7240e-010
   Trigger = 1.0833e-008
   Target  = 1.1606e-008

* END NON-GRAPHICAL DATA
*
```

Fig. 6. Proposed Flip Flop- Delay

Delay of this method achieved is about 0.7ns. The output of power consumed by the proposed power gated TSPC flip flop is illustrated in fig. 6.

The waveform is as shown below for the proposed project.

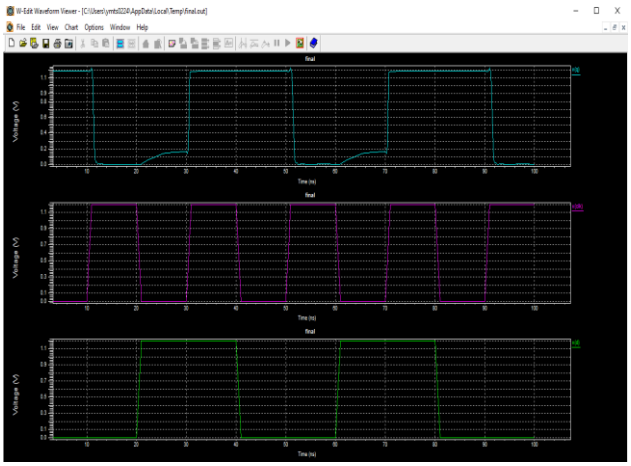

Fig. 7. Proposed waveform

The waveform of the proposed power gated TSPC flip-flop is illustrated in fig. 7.

Green color represents - D
Pink color represents - CLK
Blue color represents – Q

Comparison results of power, delay and area for existing and proposed method are illustrated and tabulated in the Table 1.

Table 1
Comparison

	Power (µw)	**Delay (ns)**	**Area (No. of MOSFET)**
Existing method	209	0.7	31
Proposed method	157	0.7	26

6. Conclusion

The design of "power gated" true single-phase clock (TSPC) based flipflops is considered in this project. Header "Power gating" concept is preferred for minimizing power utilization by switching off the connection from the potential when it is unnecessary. To save maximum power by allowing the circuit to be in ON condition as long as the required data is sent to perform the functionality, and switches OFF the power automatically when the circuit finishes the work. Since the supply is passed to the circuit only when required in the proposed D flip-flop design.

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