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Design of D Flip Flop as a Frequency Divider by Using Folded CMOS Current Mode Logic

Sahana Udupa[1*], M. Anand[2]
[1]Student, Department of Electronics and Communication Engineering, East West Institute of Technology, Bangalore, India
[2]Associate Professor, Department of Electronics and Communication Engineering, East West Institute of Technology, Bangalore, India

***Abstract*: This project presents a fixed frequency divider built on FMCML flops. Since common-mode issues might develop when employing only one type of FMCML flip-flop, the idea is based on switching FMCML flops using CMOS input differential duo. Our method avoids intermediate stages by making use of Frequency divide by 16 by adopting FCMCML D Latch having complementary transistors. An adapting approach is discussed here such that it makes use of Scaler architecture with 4 NMOS having an enable pin so that it attains minimal power dissipation and reduction in overall delay.**

***Keywords*: FMCML, MCML DFF, DIV2, Frequency Divider, Scaler architecture.**

1. Introduction

When the creation of sub harmonic signals emitted by an increased frequency source is necessary, frequency dividers are used as important building pieces in plethora of elevated modulation and demodulation aforementioned. Frequency synthesizers based on the PLL, timing generators, increased subsystems speed time-interleaved mixed signal converters are examples of such devices. The deterministic frequency dividers, for example, offers a large frequency range and a topography that simply employs ordinary digital blocks. Unless exceptionally high frequencies are required, this shortens the design, facilitates remodel and use in re-composable structures, enabling them with the most widely used Scalar architecture. Most of the aforementioned uses are mixed-signal integrated circuits, which place additional demands on the frequency divider block. When engineering High-Speed ICs using traditional CMOS technology, we run into the issue of gate switching speed being limited by delay. We may reduce propagation delay times by properly designing our transistor, as greater W/L ratios result in a faster switching gate, but also a higher power utilization, as we'll see later. It is possible to achieve high-speed operation. MOS Current-Mode Logic [MA05] circuits offer genuine differential operation, low noise production, and fixed power dissipation, which means the amount of current consumed from the power source is independent of switching activity. As a result, MCML gates have been shown to be beneficial in analogue and mixed-signal integrated circuits. As a matter of fact, CMOS technology has been scaled to provide devices capable of operating at higher frequencies up to 10 Gigahertz, requiring low supply voltages of 1V or less. In order to benefit from fast switching, Low susceptibility to common-mode clutter and disruptions, quick switching, with low power-supply switching noise. With these tools, logical families are constructed depending on methodology for increased-frequency aforementioned. This makes it straightforward to integrate mechanical and electronic integrated circuits for mixed-signal applications.

2. Objectives

a) To scale down the power dissipation by making use of supportive flip flop and also circuit will be able to operate under low supply voltage.
b) For speed circuit operation by using lower frequency as possible, as higher frequency causes overheat in the circuit.
c) Speed Performance to be increased by 15% by using the new proposed method.
d) To enhance noise immunity with low sensitivity towards common mode noise also involves fast switching.
e) Parasitic Capacitance contributes to low power design also has weak bias current.

3. Methodology

D FLOP is based on the outline of a simple D-latch, that is used as the basic building block in the construction of FMCML and a master and slave arrangement (i.e., a topography constructed chaining two Level sensitive flops with counter-phase clock signals). N D Flops are employed in a 2N divider, with the output of each D FLOP being linked to the clock input of the one after it. In order to do this, it is necessary to link the input and output of a PMOS differential pair in an impractical manner.

We obtain a VCM, Imax, N type with a minimum difference of 300 mV from VCM, out, N type when using deep sub micron CMOS technique, wherein |VTH| is generally smaller than 0.35 V, the lowest Vov becomes approximately 50 mV, and a desirable VSW is worth approximately is about 600 mV. The conventional solution to this issue is to Between the DFFs, a source follower acts as a phase changer; moreover, doing so tends to increase in power use, and for efficiency in speed, the source follower's power can account for a considerable portion

*Corresponding author: sahana.udupa9696@gmail.com

of the total power utilization. This project, we provide a novel strategy where levels of every input's and output's common mode of each Individual clock dividers blocks are acceptable by swapping complimentary FMCML D FLOP phases, omitting any intermediate step. In actuality, the D-dual latches was built utilizing complimentary technology.

The D FLOP with the output provided by a NMOS/PMOS differential duo will be referred to as N type in the sections that follow. Fig. 1 reports the outlines of the N type and Fig. 2 reports the outline of P type FMCML D Flops. Here, we created a 2N generic fixed frequency divider, that is frequency divider by 16.

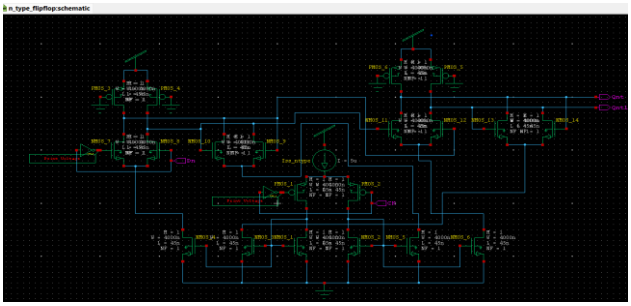

Fig. 1. Outline of N type Folded MCML Flop

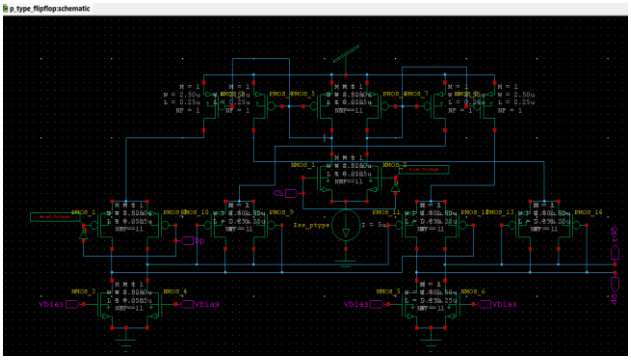

Fig. 2. Outline of P type Folded MCML Flop

The D FLOP in this particular application, which employs an INDIVIDUAL CLOCK DIVIDERS, has unitary feedback and is packed by additional D flops, moreover the input differential duo of the D FLOP is composed of supportive transistor types with regard to the driver gate. As a result, in the scenario under examination, where the driving cell is an N type INDIVIDUAL CLOCK DIVIDERS and the load cell is a P type INDIVIDUAL CLOCK DIVIDERS, we may infer that the load is the total of two contributions. The first contribution is provided by the rail of nMOS differential duo with the slave latch inside the gate capacitance of the driving DIV2 level. The second element is provided by the gate capacitance at the CK input of the load P type DIV2 level. The capacitive at the load's P type DIV2 level's CK input. INDIVIDUAL CLOCK DIVIDERS level makes up the second contribution.

As a result, it demonstrates how the bias currents rely on the input capacitances, contain all effects that are independent of the D FLOP bias current, ISS, and N type, and described as the proportion of supportive-type the operating and loading bias currents INDIVIDUAL CLOCK DIVIDERS steps. The CK-to-Q delay of the P type INDIVIDUAL CLOCK DIVIDERS packed by an N type stage INDIVIDUAL CLOCK DIVIDERS may be calculated using the same equations by switching N type and P type.

This paper presents a unique design that uses supportive minimal voltage of N type and P type FMCML D Flops to construct fast with fixed clock dividers that are energy-efficient. Two design solutions have also been proposed as a result of a thorough examination of the FMCML flip-flops propagation delay, the first of which aims to achieve the smallest PDP and the second of which aims to obtain the greatest speed performance.

4. Implementation

This project is implemented by using Tanner EDA tool. The role of EDA tool is to help design and verify a circuit's operation by numerically solving the differential equations describing the circuit.

A. Software Requirements

- S-Edit (Simulator Edit)
- Circuit Emulator T-Spice
- W-Edit (Waveform Edit)
- L-Edit (Layout Editor)

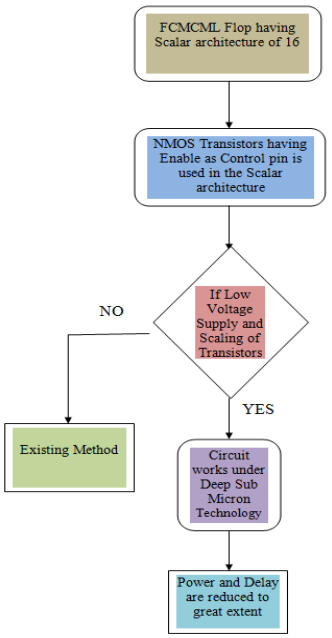

Fig. 3. Flow Chart of Proposed Method

The fig. 3, depicts the flow chart of the proposed method.

It summarizes the implementation of FCMCML flops when compared to MCML D Latch. In this method we make use of Scalar architecture with 4 NMOS having an enable pin at the gate which is used as a control pin, as our main target is to minimize the power and delay. The added advantage is having a low voltage supply of 0.8V and also scaling of transistors are performed in order to make the circuit work under deep submicron technology which helps in the reduction of power and delay to a greater extent.

Schematic Editor (S-Edit) is a user-friendly using a PC schematic capture design environment. It possess the power to manage the most challenging customized designed IC design capture. S-Edit gives you the ability to explore design decisions and offers a simple way to see the results of those decisions. You have greater freedom to transition to an ideal solution when the design cycle is shorter, which leaves additional resources and time for protocol bottleneck verification. Lower risk further downstream, greater yield and faster time to market are the outcomes. S-Edit provides outline capture for one of the most intricate fully customized IC design, has powerful and ease of use interface, and also economical.

5. Results

The results of above proposed method of FCMCML flip flop are discussed in this section, The below Fig. 4 depicts the outline of proposed N type MCML flop, it means the CK and CK bar are made of P type flop and the input D is made of N type flop

Case 1: Parameter CK is subjected to 0 and the transistor near CK are turned on whereas, the transistor near D are off, the transistor connected to VDD are always turned on

Case 2: Parameter CK is subjected to 1 and the transistor near CK are turned off restricting the flow of voltage and the transistor near D are turned on which allows the data to be passed

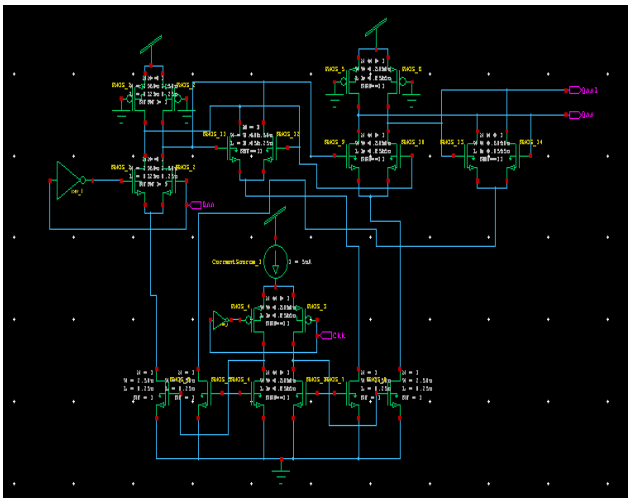

Fig. 4. Outline of N type Implemented Folded MCML flop

By using these types, we can generate a fixed frequency by using the frequency divider technique which is having value of 2^N we use N=4 that is 16.

The fig. 5 depicts the outline of proposed N type MCML flop, it means the CK and CK bar are made of N type flop and the input D is made of P type flop

Case 1: Parameters CK is subjected to 1 and the transistor near CK are turned on the transistor near D are off, the transistor connected to VDD are always turned on

Case 2: Parameter CK is subjected to 0 and the transistor near CK are turned off restricting the flow of voltage and the transistor near D are turned on which allows the data to be passed.

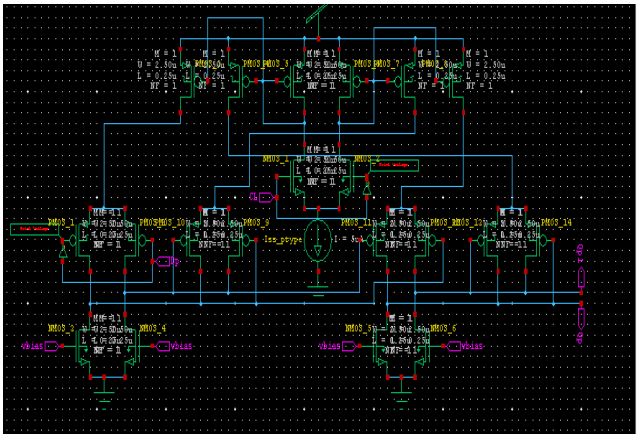

Fig. 5. Outline of P type Implemented Folded MCL flop

The fig. 6 depicts the outline of Frequency divider technique with the few advancements made as shown in the below figure.

The NMOS transistors with an enable pin is used to control the loss of power and also helps in reducing the delay keeping the aspect ratio unchanged. This technique present in the MCML latch helps in consuming less voltage as it divides and supplies the voltage to the whole circuitry.

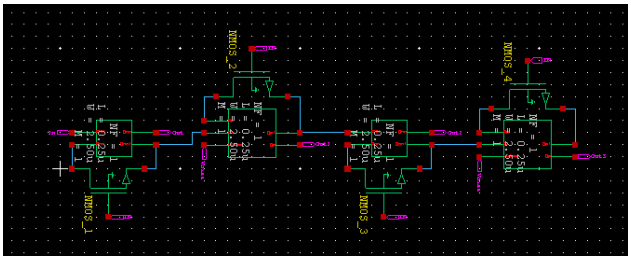

Fig. 6. Outline of proposed frequency divider in FMCML by controlling input of flop

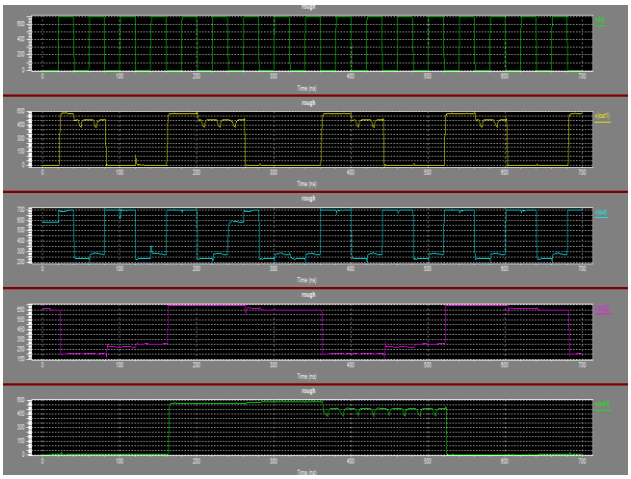

Fig. 7. Waveform Output of proposed frequency divider in FMCML

The fig. 7, depicts the final waveform obtained after the completion of the simulation process.

In the below figure, we can observe 5 waveforms visualized in 5 different colors.

Green color waveform represents the main voltage of 0.8V.

Yellow color waveform represents the voltage divide by 2 of 0.4V.

Blue color waveform represents the voltage divide by 4 of 0.2 V.

Purple color waveform represents the voltage divide by 8 of 0.1V.

The last waveform represents the voltage divide by 16 of 0.025V.

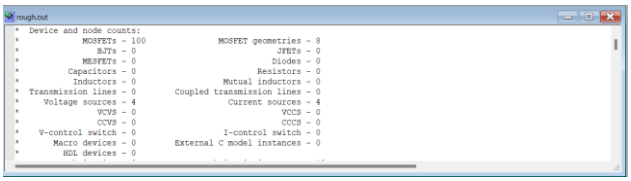

Fig. 8. Area output of the proposed method

The fig. 8 depicts the output in terms of area where we can observe a slight increase in the area by 4 MOSFET and this is due to the introduction of 4 transistor in the Scalar architecture which is used to control the power and delay factors.

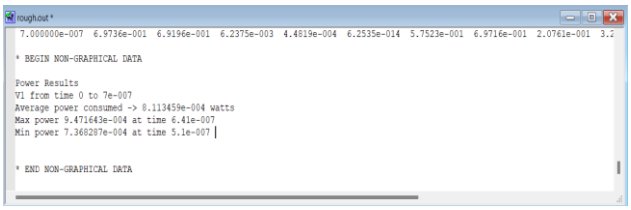

Fig. 9. Power output of the proposed method

The fig. 9, depicts the output in terms of power where we can observe the average power, maximum power and minimum power consumed for the circuit in terms of W.

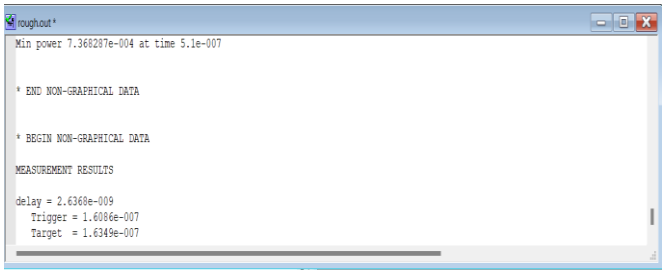

Fig. 10. Delay output of the proposed method

The fig. 10, depict the output obtained in terms of delay where we can observe the total delay in a circuit and the time take for triggering the transistors and the time taken to obtain the output in terms of second.

Table 1
Output comparison

Parameters	Existing Results	Proposed Results
Area	96 MOSFET	100 MOSFET
Power	Avg = 0.9999147mW Max = 0.118223mW Min = 0.8964584mW	Avg =0.8113459mW Max = 0.9471643mW Min = 0.7368287mW
Delay	6.6386ns Trigger=0.10900ns Target=0.17539ns	2.6368ns Trigger=0.016086ns Target=0.016349ns

The table 1, depicts the comparison table of existing and proposed method outputs.

As we can observe the reduction in power and delay in our proposed method and 0.1% increase in the area when compared to the existing method. The power is reduced by 0.1888mW and delay is reduced by 4ns which helps in speedy operation of the circuitry and also has an advantage of low voltage supply of 0.8V.

6. Conclusion

By making use of Folded MCML using P type and N type flip flops the proposed architecture is able to operate with a low supply voltage compared to MCML based architectures. Due to the scaling of transistors, the proposed circuit is able to work under Deep Sub-micron technology. By using supportive flip flops there is also a reduction of common mode problems and minimum power dissipation. The clock control is also achieved by using constant current source. By this, the propagation delay is also reduced. Due to these advantages, these are mostly used at high frequency aforementioned, clock generators, phase locked loop circuits and radio aforementioned.

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