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FPGA Implementation of Lossless ECG Compression Algorithm

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***Abstract*: A FPGA implementation of an efficient loss-less ECG compress scheme for binary encoding the data, which conserves storage space and compress the transmission time. So, the convenience has been grabbed by executing the functioning memory-less design at a peak clock rate in FPGA. ECG compression algorithm consisting dual roles:1) Adaptive Linear Prediction technique. 2) Golomb Rice coding. A systematic FPGA execution of compressed algorithm have been dispensed. To increase a interpretation, a prefer Xilinx tool uses a bitwise operation as a renewal for a distinct arithmetic operations. Proposed System shows that this design low Area & Delay architecture. This scheme is developed in Verilog HDL and simulated by Modelsim 6.4 c. To achieve synthesis of Spartan3 FPGA tools from Xilinx ISE 13.2 is used.**

***Keywords*: FPGA tool, ALP, Golomb rice coding, Xilinx, Modelsim.**

1. Introduction

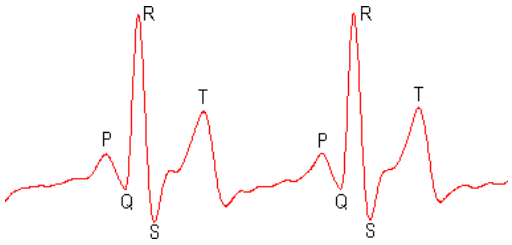

Fig. 1. ECG signal

In the last few years, the cardiovascular disease (CVD) is the main cause of death all over the world, so to detect this illness

Electrocardiogram (ECG) signal is used. Which contains valuable information about the heart state, where Fig. 1 shows the ECG signal where P, QRS and T wave indicates depolarization of atria, depolarization of the ventricles and repolarization of the ventricles respectively. When tracking ECG signal it contains huge amount of data, hence there is need of more space. In this presented design we use loss-less ECG compression technique to save storage space.

2. Literature Survey

A. Survey Paper 1

In 2018, Tsung-Han Tsai, Wei-Ting Kuo, An Efficient ECG Lossless Compression System for Embedded Platforms with Telemedicine Applications. Using compression algorithm, they have got the compression ratio of 2.84x and 2.77x on MIT/BIH arrhythmia of two-level data base. This design ensures high performance but there is a more timing delay.

B. Survey Paper 2

In 2018 A Hybrid Data Compression Scheme for Power Reduction in Wireless Sensors for IoT, Chacko John Deepu, Chun-Huat Heng, and Yong Lian. Here while doing compression there be losses of more data. To enable transmission mode we use two technique that is lossy and lossless technique.

3. Methodology

ECG compress algorithm consists of three parts: ALP technique, Golomb rice coding and Data packing module, where they performs as a prediction part, entropy coding part and compressed bit stream respectively.

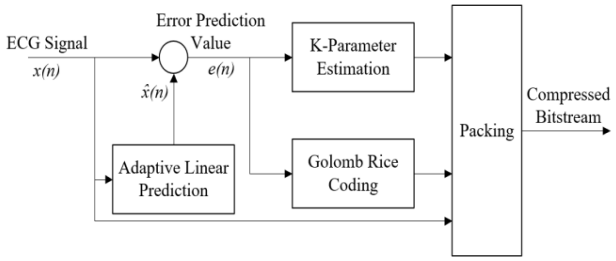

Fig. 2. Block diagram of proposed system

A. Adaptive Linear Prediction

It is proposed that an ALP approach be used for enhance prediction error by holding the value as low as possible. The prediction value is estimated using the previous four samples. The following equations are used to calculate the value of the four:

D1_2 (n) = x (n-1) – x (n-2) ----------(1)
D1_3 (n) = x (n-1) – x (n-3) ----------(2)
D2_3 (n) = x (n-2) – x (n-3) ----------(3)
D3_4 (n) = x (n-3) – x (n-4) ----------(4)

To account for the essential quality of the ECG signal, with coefficients the simple differential predictor are used. The following differential predictors were chosen in algorithm

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development because to their cheap computational cost and strong performance in predicting prediction value. A full discussion of the equation is as follows,

P1: $\hat{x}$ (n) = x (n-1) ----------(5)

P2: $\hat{x}$ (n) = 2x (n-1) - x (n-2)----------(6)

P3: $\hat{x}$ (n) = 3x (n-1) - 3x (n-2) + x (n-3)-----(7)

Every clock cycle for the ALP block, 11-bit input is handled. As explained in the suggested original algorithm, linear prediction is conducted differently for the first four inputs than for the subsequent inputs. As a result, two separate linear predictors are created. A control unit is shown in Fig 3 regulating the input data by generating control signals for selecting the linear prediction unit and delivering data from linear prediction units to the error predictor. Simple arithmetic is used in the error predictor to determine if the number is greater than zero or lesser than zero.

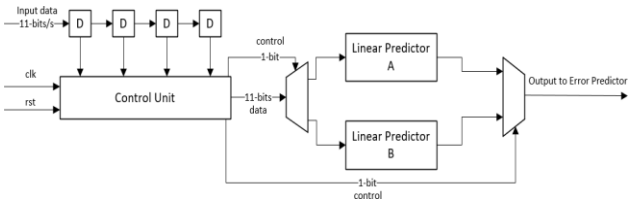


Fig. 3. Architecture of ALP

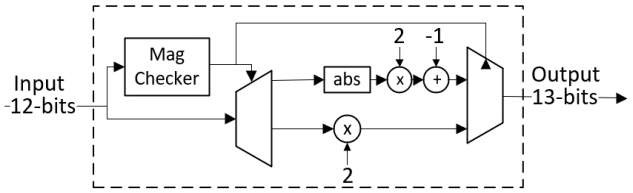


Fig. 4. Block diagram of error predictor

The linear prediction module provides input data to the error predictor. Figure 4 depicts the hardware architecture for the error prediction module. A sign bit is checked during ALP processing to determine if number is positive or negative.

B. Golomb Rice Coding

Golomb coding is an entropy-based data compression algorithm. It is divided into: quotient and remainder, indicated the letters as U and V, respectively.

quotient: M[n]; This is encoded with a unary code

remainder: M[n]mod 2k; This is encoded with a binary code

where, M[n] is a positive integer, and k is the remainder for the number of bits. The value M[n] is obtained by converting a negative prediction error into a positive number.

Golomb rice coding is the most difficult and time-consuming phase of the entire compression technique. In Golomb Rice coding, the hardware design is meant to maintain the data.

The predicting error module's post-processed data is used as input data. Because data is processed for a single window, a 40x13-bit register is used to store the values of a single window When new window values arrive, the value of U and V, which stand for quotient and remainder, respectively, is determined by analysing previous window values. As illustrated in Fig. 5, the architecture of this module can be separated into two parts: data regulating and computing. To reduce the processing time, operations have been separated into distinct clock- cycle in the computing section. Bitwise operation has being used already to conduct multiplication, power, mod, and division operations instead of in-built operative of division and power. The design can benefit from a reduction in the number of gates and power usage by employing this bit shifting.

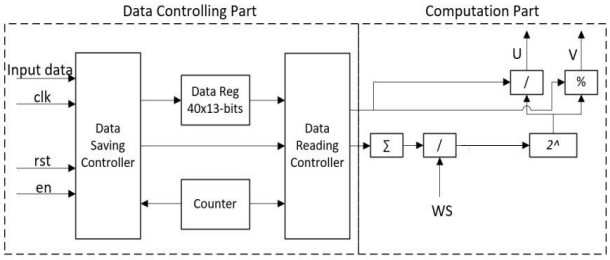


Fig. 5. Block diagram for Golomb rice coding

C. Data Packing Format

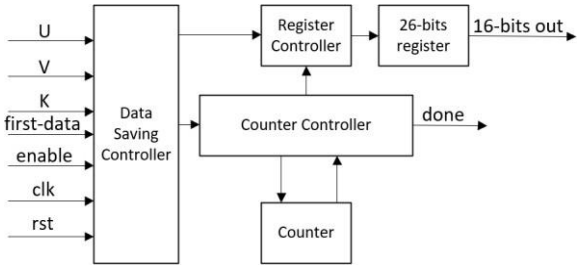


Fig. 6. Block diagram of packaging module

The initial sample of 11-bit ECG data, as well as the k parameter with three bits for single window and prediction error, are encoded using Golomb-Rice code in the decoding phase to reproduce the original signal. Figure 6 depicts the generated bit stream. Two controllers in the packaging module are in charge of saving data in a temporary 26-bit register and delivering. When sixteen or more bits are keep reserved in the non-permanent register, the output data is 16 bits.

4. Results

A. Analysis of the Result Obtained During Simulation and Synthesize

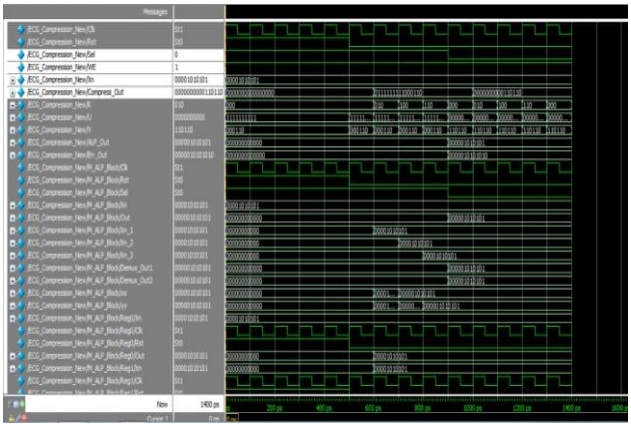
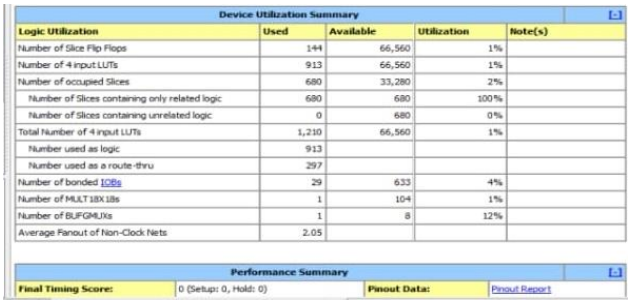


Fig. 7. Output waveform of simulation process

Input(a):1010101
Compressed Output(b):110110



Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	144	66,560	1%	
Number of 4 input LUTs	913	66,560	1%	
Number of occupied Slices	680	33,280	2%	
Number of Slices containing only related logic	680	680	100%	
Number of Slices containing unrelated logic	0	680	0%	
Total Number of 4 input LUTs	1,210	66,560	1%	
Number used as logic	913			
Number used as a route-thru	297			
Number of bonded IOBs	29	633	4%	
Number of MULT 18X 18s	1	104	1%	
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	2.05			

Performance Summary

Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report

Fig. 8. Device utilization report

The device usage summary of an ECG compressed out is shown in the fig. 8, where the number of LUT's occupied by this device is 913, the delay of this system is 7.165ns.

The below figure shows power analysis of the proposed system; thus, the obtained power is 33.8mW.

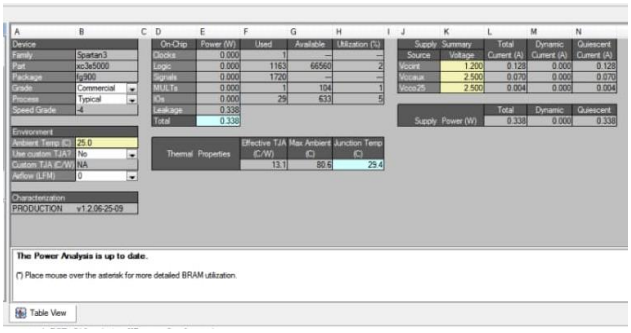


Fig. 9. Power analysis report

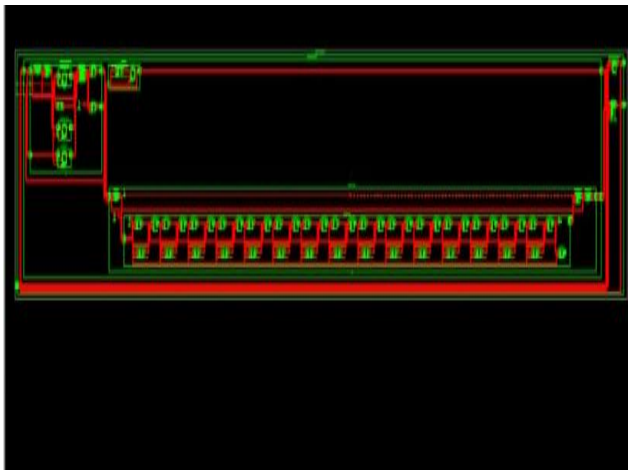


Fig. 10. Technology schematic view

Table 1
Obtained result

Parameters	Proposed Result
Compression Ratio	1.57
Number of LUT's	1210
Number of slices	680
Delay	7.165 ns
Power	33.8 mW

5. Conclusion

A lossless compression algorithm based on an adaptive linear prediction and Golomb rice coding approach is devised in this research, with a compression ratio of 1.57. It compresses data without causing any loss of the original data. The suggested algorithm and hardware implementation use the least amount of power and area when compared to existing methods.

6. Future Scope

For the time being, this proposed ECG compression algorithm will be employed for data compression. It will be utilised in image compression in the future. For a high-speed medical application, it will be implemented on real-time FPGA hardware.

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