International Journal of Research in Engineering, Science and Management
Volume 5, Issue 6, June 2022
https://www.ijresm.com | ISSN (Online): 2581-5792

Implementation and Analysis of Wallace Tree Multiplier Using Kogge Stone Adder and Sklansky Adder

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***Abstract*: Multiplier is the most dominant block in DSP systems, Embedded and VLSI applications. So, it is necessary to design a multiplier which provides high performance. Power consumption, area occupied and delay are the key features which determines the performance of a multiplier. When the process of multiplication is initiated, it gives rise to partial products and it also necessitate to sum the partial products to carry out this process half adder and full adder is used, which takes more time and area for calibration. This paper mainly focuses on implementation of 16X16 bits multiplier using Wallace tree approach with 15-4 compressor. The partial products are compressed using 5-3 compressor along with half adder and full adders. In the enclosure stage parallel prefix adders such as Kogge Stone adder and Sklansky adder are utilized for the partial product addition. The obtained results of both multipliers are compared, and analyzed that Sklansky adder is better in terms of area (Number of LUT's).**

***Keywords*: Wallace tree multiplier, 15-4 Compressor, Kogge Stone adder, Sklansky adder, Area, Delay.**

1. Introduction

Multiplier circuit is the vital technology behind the high performance of the various electronic systems such as digital signal processors, digital image processing, microprocessors, microcontrollers and so on. Among arithmetic operation like addition, subtraction, multiplication, division, the most often used operation is addition and multiplication in electronic system. Its feature is to provide high-speed, truncate power consumption and area. Various algorithms for multiplication process are presented like booth algorithm, modified booth algorithm, Wallace tree algorithm and so on., using these algorithm multipliers are designed. The modified booth algorithm is approachable as it generates a smaller number of partial products for addition purpose. In VLSI we need a multiplier which is favourable in tip-off operational speed hence Wallace tree multiplication algorithm is more preferred. By furtherance of VLSI technology, the circuit need to operate with pulled off excessive speed and shorten by the area. In sequence to improve the speed of Wallace tree multiplier without devaluing specification of area, a new configuration of Wallace tree multiplier is presented. In the presented design, in the enclosure stage of partial products summation is carried out by prefixed parallel adders (PPAs). Here, Wallace tree multiplier system is design using Kogge stone adder and Sklansky adder where the reduction is done with an aid of 15-4 approximate compressor. Multipliers are implemented using Verilog HDL in Xilinx design suite. The presented designs are simulated in Modelsim 6.4 simulator and synthesized using Xilinx ISE 14.7 synthesizer, and are examined in remark of area (No. Of LUTs) and delay (ns). The simulation results for 16-bit multipliers using Sklansky adder in tip-off area and delay are contrasted with the multiplier which is designed in aid of kogge stone adder. The obtained results are analysed and implemented on the Spartan 3 FPGA tool.

2. Literature Survey

A. *Survey Paper 1*

In 2018, Ayyagari Sai Ramya, came up with a carry save algorithm for designing the multiplier with Wallace tree perspective. B.S.S.V. Ramesh Babu, interprets that preferred model not just intimates high speed but also there would be a reduction in terms of delay. The hindrance of this design is that it tenants withal energy along with additional area.

B. *Survey Paper 2*

R Agnes Lilly, propound the design of 32 bits multiplier with KSA and the acquired outcomes of this multiplier is analogized with the parallel adder, it is manifested that better enhancement is secured in tip-off area and delay. The parallel adder dispenses less exactness and the compressor outline is more complicated.

3. Methodology

A. *Multiplier*

"ADD and SHIFT" is the algorithm followed by most of the multiplier. Multiplier is a circuit used to multiple any two binary numbers.

For example: A=1010, B = 1111

1 0 1 0 ------ Multiplicand
1 1 1 1 ------ Multiplier

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```
    1 0 1 0 ┐
  1 0 1 0   │  Partial
1 0 1 0     │  products
  1 0 1 0 ──┘
1 1 1 1 1 1 0------- Result
```

A 16 x 16 bits multiplier is implemented, while multiplying these 16 bits many partial products are generated i.e.,256 bits. The final stage of multiplication process is addition where 32 bits are obtained. When add and shift algorithm is followed to multiply higher number of bits, it's a time-consuming process and more delay is secured. Hence a different algorithm approach is used that is Wallace tree approach in this presented paper.

B. Wallace Tree Approach

A Wallace tree approach architecture was implemented by Chris Wallace in the year 1964. Any two integers can be multiplied using this approach where, many partial products are generated. To abate this partial product, compressors such as appropriate or accurate compressors can be used, to obtain the better outcomes in order of area and delay here in the propound multipliers approximate 15-4 compressors is used.

The stages of Wallace tree approach are,

- Multiply each bit of A integer with the set of B integers
- The number of partial products is decreased to two using approximate 15-4 compressor.
- AXB integers are clumped in two numbers, and the addition is carried out with a traditional adder.

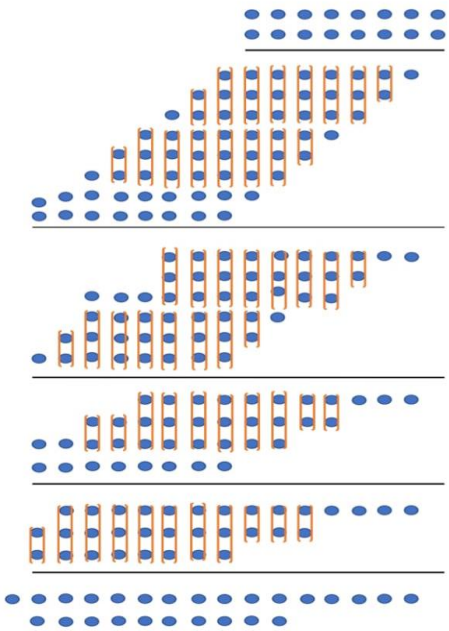

Fig. 1. Wallace tree approach

C. Approximate 15-4 Compressors

As the name intimate, it renders as near as damnit output and it internally comprises of two 5-3 compressors and full adders. 15-4, intimates that 15 inputs are provided to full adder, after compressing the data that is from 15 bits to 4 bits the outputs are sent through 5-3 compressors. The mantle of this compressors is to reduce the partial products generated during multiplication process and prone to prefixed parallel adders for addition process. These compressors portray an imperative role in digital image processing for image and video compression.

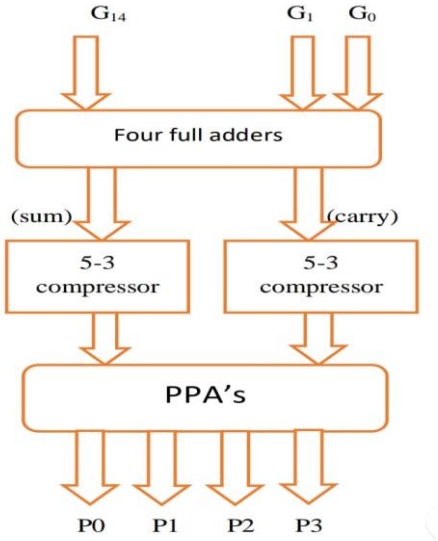

Fig. 2. Flow diagram of an 15-4 compressor

4. Wallace Tree Multiplier Using Koggestone Adder

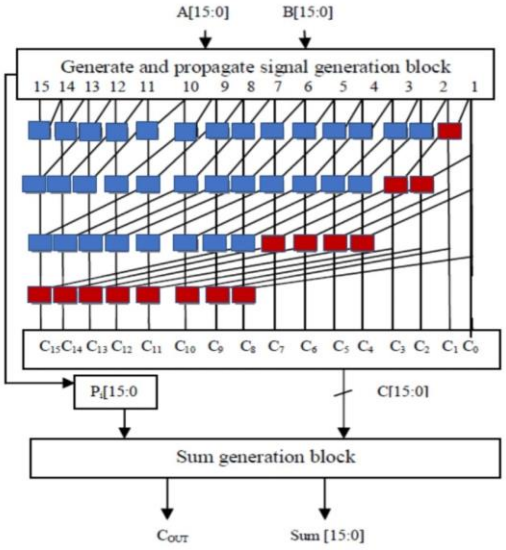

Fig. 3. Architecture of a Kogge Stone adder

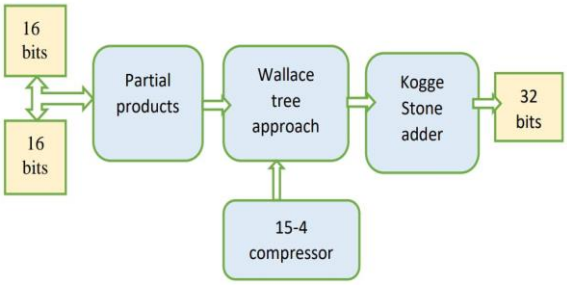

Fig. 4. Block diagram, Wallace tree multiplier where Kogge Stone adder is used to perform last stage addition

Kogge stone adder is considered as one of the main adders among the parallel prefix adders because of its high-speed performance and lower fanout. but the problem lies in its internal wiring profusion, so it holds more area for partial product addition and there will be increase in delay when compared to others parallel prefix adders. The delay of the structure is given by log2n with [n(log2n)-n+1] computation nodes.

Three different stages during computation:

- Pre-Processing stage:
  Pi = Ai XOR Bi
  Gi = Ai AND Bi
- Generation of carry
  Gi = (Pi AND Gi*) + Gi
  Pi = (Pi AND Pi*)
- Final processing stage:
  Ci = Gi
  Si = Pi XOR Ci-1

5. Wallace Tree Multiplier with Sklansky adder

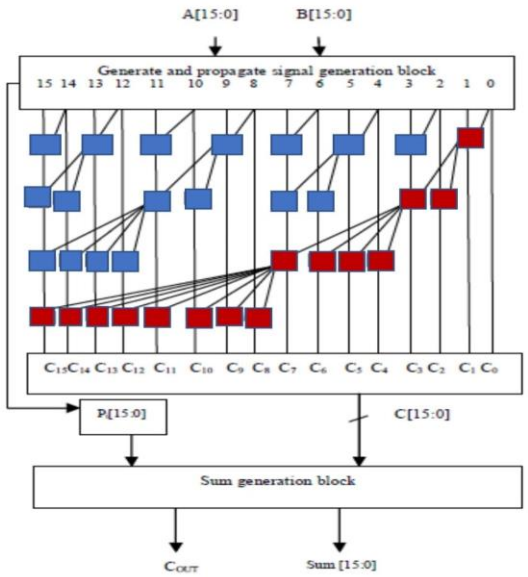

Fig. 5. Architecture of an Sklansky adder

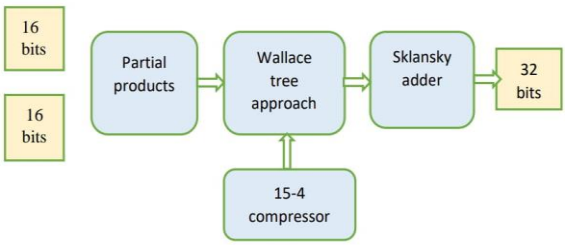

Fig. 6. Block diagram of a Wallace tree multiplier where Sklansky adder is used to perform final stage addition

The structural of Sklansky adder is unadorned and systematic, it is not so intricate as kogge stone adder. The Sklansky adder follows the divide and conquer structure rule. The prefixes of this structure are recursively computed into groups like two, four, eight and sixteen bits so on though the logic depth of the Sklansky adder is minimum, it has high fanout. As a fanout vastly extend from inputs to outputs this engender to colossal amount of latency. The structure of Sklansky adder shows that it conquers slighter area with contrast to kogge stone adder. The delay of the structure is given by log2n with [n/2 log2n] computation nodes.

Different stages during computation:

- Stage I:
  Gii = Ai AND Bi
  Pii = Ai OR Bi
- Stage II
- Pij = P_{ik} AND P_{k-1j}
- Gij = G_{ik} OR Pik G_{k-1j}
- Stage III
  Ci+1 = Gi OR (Pi AND Ci)
  Si = (Ai XOR Bi) XOR $G_{i-1:-1}$

6. Results

A. Analysis of the Result Obtained during Simulation and Synthesize

The paper presents an 16X16bit Wallace tree multiplier system with two different parallel prefix adders such as kogge stone adder and Sklansky adder. The multipliers which are implemented is simulated in modelsim 6.4a and synthesized with Xilinx ISE 14.7/13.2 by using Verilog HDL.

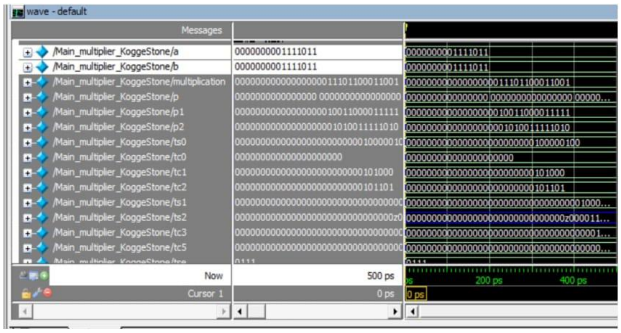

Fig. 7. Output waveform of simulation process (multiplier with Kogge Stone adder)

Input (a) = 0000000001111011
Input (b) = 0000000001111011

Output (Multiplication)
= 00000000000000000001111011000011001

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	632	7,168	8%
Number of occupied Slices	343	3,584	9%
Number of Slices containing only related logic	343	343	100%
Number of Slices containing unrelated logic	0	343	0%
Total Number of 4 input LUTs	632	7,168	8%
Number of bonded IOBs	64	97	65%
Average Fanout of Non-Clock Nets	3.32		

Fig. 8. Estimated values of 16 bits wallace tree multiplier with kogge stone adder

The device usage summary of a wallace tree multiplier with kogge stone adder is shown in the above figure, where the number of LUT's occupied by this device is 632. The delay of this system is 68.722 ns (nano seconds).

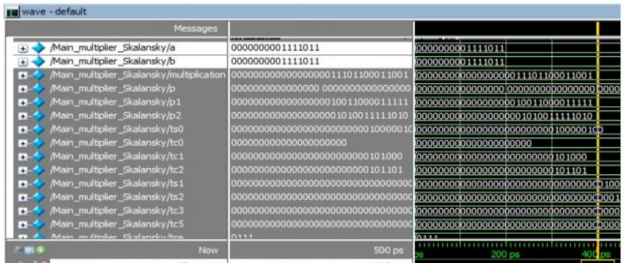

Fig. 9. Output waveform of simulation process (multiplier with Sklansky adder)

Input (a) = 0000000001111011
Input (b) = 0000000001111011

Output (Multiplication)
= 00000000000000000011101100011001

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	615	7,168	8%	
Number of occupied Slices	339	3,584	9%	
Number of Slices containing only related logic	339	339	100%	
Number of Slices containing unrelated logic	0	339	0%	
Total Number of 4 input LUTs	615	7,168	8%	
Number of bonded IOBs	64	97	65%	
Average Fanout of Non-Clock Nets	3.29			

Fig. 10. Estimated values of 16 bits wallace tree multiplier using Sklansky adder

The device usage summary of a wallace tree multiplier with Sklansky adder is shown in the above figure, where the number of LUT's occupied by this device is 615. The delay of this system is 67.54 ns (nano seconds).

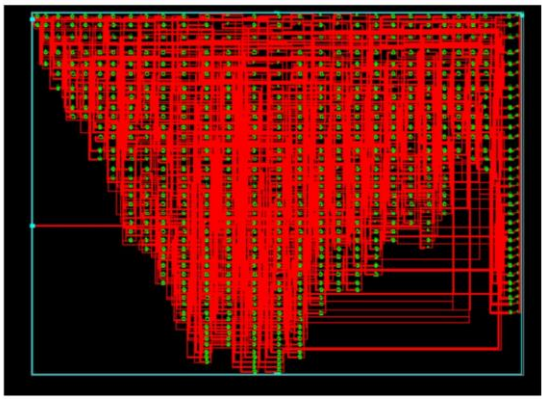
Fig. 11. Technology schematic view

B. *Implementation Results*

The obtained results are executed on a (SPARTAN 3 XC3 S200TQ144) FPGA tool.

Input A [15:0] =0000000001111011
Input B [15:0] =0000000001111011
Output [31:0] =00000000000000000011101100011001
Select line 00=00000000(output), Fig 12(a)
Select line 01=00000000(output), Fig 12(a)
Select line 10=00111011 (output), Fig 12(b)
Select line 11=00011001 (output), Fig 12(c)

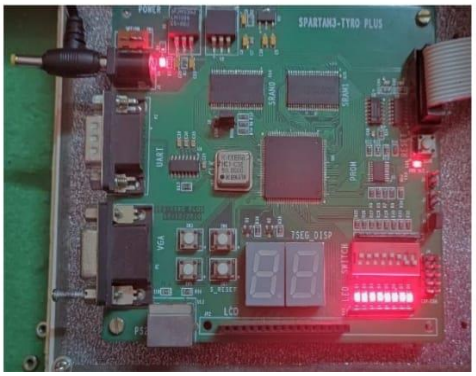

Fig. 12(a). The multiplication output obtained, when the select line is 00 and 01

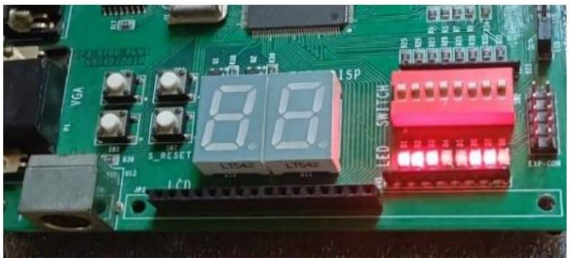

Fig. 12(b). Output secured when the select line is 10

Fig. 12(c). Output obtained when the select line is 11
Fig. 12. The results obtained during the hardware implementation. LED ON indicates the output is 0 and LED OFF shows the output is 1.

C. *Comparison Table*

Table 1
Comparison of a Wallace Tree Multiplier using Koggestone Adder and Sklansky Adder

Parameters	**Wallace Multiplier Using Koggestone Adder**	**Wallace Multiplier Using Sklansky Adder**
Number of LUT's	632	615
Number of bounded IOB's	64	64
Delay	68.722ns	67.54ns
Number of logic level	40	39

The Wallace tree multiplier with the aid of two different parallel prefix adders that is Kogge Stone adder and Sklansky adder is compared in terms of different parameters like Number of LUT's Number of bonded IOB's, Delay, Number of logic level. where the multiplier with Sklansky adder occupies a smaller number of LUT's and delay that is 615 and 67.54 ns.

While the multiplier with kogge stone occupies 632 LUT's and the delay is 68.722 ns.

7. Conclusion

Two different Wallace tree multiplier structure are analysed here with contrasting parallel prefix adders one with Kogge Stone adder, and the another with Sklansky adder. Where, both this Wallace tree multiplier structure are simulated in model sim 6.4 and synthesized with Xilinx 14.7. The obtained results are implemented on a Spartan 3 FPGA tool and the outcome is compared in terms of delay and area (number of LUT's). It is concluded that the multiplier with Sklansky adder provides better results in terms of number of LUT's and delay when compared to the multiplier using kogge stone adder.

8. Future Scope

The implemented Wallace tree multipliers can be comprehensively utilized in FIR filter, where these filters are most extensively used device in Digital system processing applications, like audio system, control system and medical devices etc. multiplier circuit to use it for the applications like multimedia, Robotics,3D graphics, medical devices, audio system and control system etc.

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