International Journal of Research in Engineering, Science and Management
Volume 5, Issue 5, May 2022
https://www.ijresm.com | ISSN (Online): 2581-5792

Design and Analysis of Nanoscale Two Stage OTA

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***Abstract*: This electronic document describes the implementation of a CMOS two-stage OTA in the Nanoscale technology. There are various approaches to design the amplifier circuit viz. a traditional approach of designing OTA using pole-zero, gain bandwidth, slew rate, loading effect information and calculating the aspect ratios of MOSFET. Another approach is the method of approximation concerning the design theory. Most of the electronic devices consume large area and power which is undesirable. Hence it is important to reduce the size and power consumption. Designing analogue circuits not only requires a rethink of the typical architecture of OPAMPs and OTAs regarding the number of stacked transistors to avail maximum swing but also it requires the attention on necessary inversion level of the MOS transistors to support lower supply voltages and optimum voltages and optimum power-performance level.**

***Keywords*: CMOS, OTA, optimization, advancements.**

1. Introduction

Most of the electronic devices consume large area and power which is undesirable. Hence it is important to reduce the size and power consumption. Designing analogue circuits not only requires a rethink of the typical architectures of Op- Amps and OTAs regarding the number of stacked transistors to avail maximum swing but also it requires the attention on necessary inversion level of the MOS transistors to support lower supply voltages [1], optimum voltages and optimum power-performance level.

The aim of this project is to design and implement a two-stage Operational Trans-conductance Amplifier (OTA) using Nano scale CMOS technology. It is desired to have enhanced gain which is achieved with the help of a voltage combiner as it helps in boosting the gain of the pseudo differential stage at a reduced power consumption level, although the bandwidth is limited [1]-[2].

Mentor Graphics tool was used after implementing the design on NgSpice software. Mentor Graphics is not user-friendly, but it provides information about the region of operation of MOSFETs and the drain, source and gate voltages. In NgSpice we can simulate any model by downloading and including the file from predictive transistor models whereas we have to buy model packages for mentor graphics.

The voltage combiner aids in boosting the gain of the pseudo differential stage at a reduced power consumption level, although the bandwidth is limited. The technique needs to be analysed mathematically and should be matching with the simulated results.

2. Low Power OTA

A. Definition

Operational trans-conductance amplifiers (OTA) coming under class AB amplifier category are devices that convert an input voltage to an output current. They are primarily voltage-to-current amplifiers. Unlike traditional operational amplifiers or op-amps, OTAs represent a voltage-controlled current source (VCCS). Their transconductance parameter is controlled by an external, amplifier-bias current and expressed as a function of the applied voltage.

B. Nanoscale Design

Nano science is a phenomenological study at length less than 100nm. Products created with building blocks at a length scale of less than 100nm is termed as Nano technology. Nano electronics is one of the most mature of the Nano technologies [3].

The Nano scale Design studies are based on two ideas. One is shrink-down subtractive photolithography, and another is atoms-up or additive photolithography also called as a disruptive technology. Electronics deals with the shrink down technology for technology shrinkage. There are two types of CMOS scaling techniques:

1. Constant Field Scaling
2. Constant Voltage Scaling

To reduce power consumption as well as the device dimensions, Constant Field Scaling is used to scale down the device parameters and also to enhance the productivity of a particular device. The design requirements are fulfilled by 130nm PTM technologies which give the minimum required voltage for functioning to be 1.3V as V_{dd}-V_{ss}. The supplied voltage goes on reducing from 130nm to 32nm, depending on the threshold requirements of the NMOS and PMOS transistors of a given channel length.

The Nano scale design also has its drawbacks such as the channel length modulation. Moreover, the technology has reached to still obtain the desired output level for a smaller chip area and thus reducing the power dissipation and material requirements. Fig. 1. shows the perspective of design length of transistors, and it's evolution, also compares the technologies with that of the biological components which can be seen in day to day life so far [4], [5].

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100m			
	Trees	Cellphone Tower	Macro Tech
	Human Being	Server	
	Human Brain	Mother Board	
100mm			
	Human Heart	Packaged Chip	Meso Tech
	Human eye ball	Microprocessor	
	Human Retina	Cache Memory	
100μm			
	Human Hair	ALU	Micro Tech
	Human Arteries	Multiplier	
	RBCs	Logic Gate	
100nm			
	Cell Nucleus	Gate Length	Nano Tech
	DNA	Gate Oxide	
	Carbon Atom	Silicon Atom	
100pm			
	BIOLOGICAL	ELECTRONICS	

Fig. 1. Perspectives of design length

C. OTA

With the scaling of OTA transistor, we have got the Nanoscale design of the circuit at channel lengths of 32nm, 45nm, 65nm, 90nm and 130nm. The OTA is nothing but a voltage combiner which accepts inputs from gates of transistors M1 and M2 shown in the fig. 2. The input supplied to the transistors for ac operations are found out by operating point analysis and they are lying in between 0 and

-150mV for different channel lengths. The transistor sizes are chosen to avoid short channel effects in Nano scale implementations. The length of the transistors is taken three times that of the models provided by PTM [6].

An attempt has been made to obtain a higher gain at the low power supply and least power dissipation. Not only the OTA is implemented, but also the external effect (Temperature) is considered.

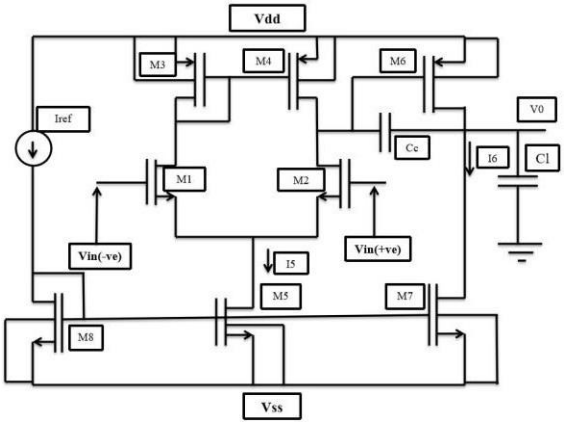

Fig. 2. OTA circuit

Design parameters that have been considered while designing the OTA include Gain Bandwidth (GB), Input Common Mode Range (ICMR) through operating point analysis, Load Capacitance (Cl), Slew Rate (SR) [5].

Design steps adopted by us include the following equations:

The compensating capacitor is 0.22 or greater than the load capacitor to satisfy the pole-zero placements.

i.e. $Cc>0.22*Cl.$ (1)

Next step is to determine the minimum value of current tail I5 in the circuit to keep the reference current source same as the tail current, and it depends upon the compensating capacitor and the slew rate.

$$I5=SR*Cc \quad (2)$$

The aspect ratio of transistors are determined by respective current crossing through it and also on the voltage required to keep it in saturation. In nano-scale regime the existing methods and equations used for microscale design did not work and the values of aspect ratios need to be nearly approximated by starting the circuit itself from scratch. Right from the design of current mirror on the tool adopted with the given technology file. The values of aspect ratios of transistors were chosen practically by doing stepwise simulations from current mirror to first stage amplifier and then the second stage. This value is also affected by the oxide thickness (tox) and also on the mobility of charge carriers of particular MOSFET [6], [7].

The Theoretical Gain of the amplifier can be given by:

$$A_V = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2+\lambda_3)I_6(\lambda_6+\lambda_7)} \quad (3)$$

Where Av is the overall gain of the two stages OTA.

λ with its subscripts is the channel length parameter of the particular transistor.

I5 and I6 are currents through the transistors M5 and M6 respectively.

gm2 and gm6 are transconductances of M2 and M6 respectively.

Theoretically it's very difficult to find the gain as λ varies in the Ids-Vds graph at different operating points.

3. Simulation Results

A sinusoidal input waveform of 0.2mVp-p is supplied at one of the inputs, i.e., Vin1 and Vin2 and output at the load capacitor is recorded. After a certain transient period, the peak-to-peak voltage is recorded, and the output for 130nm design is found out to be 200mVp-p which means a gain of 10000.

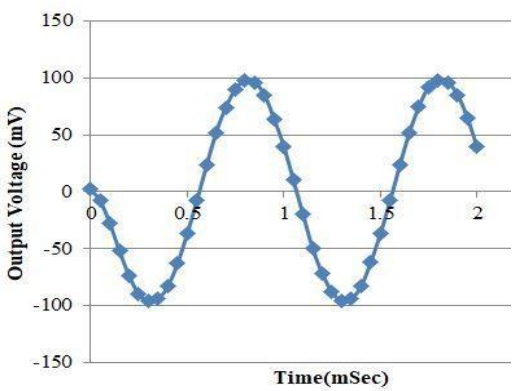

Fig. 3. Output swing of 130nm OTA

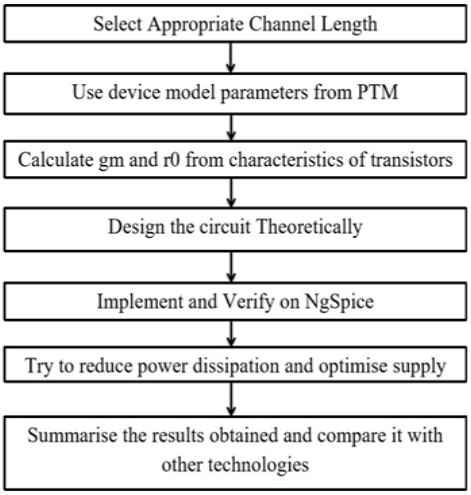

Fig. 4. Algorithm for OTA design

A. *Frequency Response*

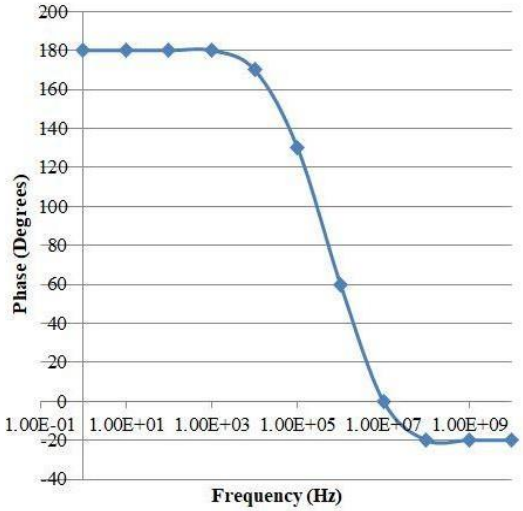

Fig. 5. Phase response

As an OTA is a class AB amplifier, the OTA works for a phase between 180 degrees to 360 degrees. The above phase diagram depicts the working of the amplifier from 180 degrees to -20 degrees for frequency range lying between 0 to 26.301Mhz.

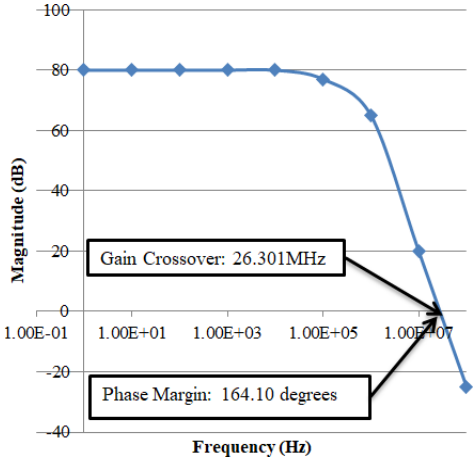

Fig. 6. Gain response

The OTA works for a certain gain crossover frequency where the magnitude of gain is 1. This gain crossover frequency is depicted in the above figure. A constant gain of 80dB is obtained for the frequency of about 10kHz.

The gain of OTA reduces as the channel length goes on decreasing. This is not just result of the transistor size but also the electron-hole mobility also called as one of the short channel effects. Sophisticated techniques are adopted to reduce all undesirable effects in the amplifier.

Effect of temperature:

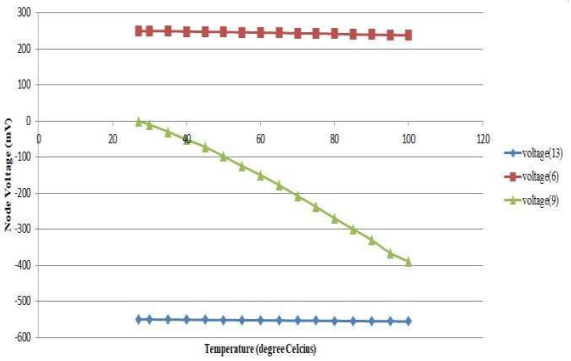

Fig. 7. Effect of temp. on node voltages

Change in temperature also affects the node voltages as the Threshold voltage is interrelated to it. The change in node voltages with temperature is depicted in the above graph. The output voltage at a common mode input of -0.1355V varies linearly from 0V at 27 degrees Celcius to -392mV at 100 degrees Celsius for 130nm model. Not only thee output voltage, but all other node voltages show a fall in node voltages. The gradient of the output voltage concerning temperature at dc analysis is found out to be equal to -5.37mV/degree C. The gradient of voltage is found out different at different nodes. The gradient decreases more towards the output side that is just the result of threshold voltage depletion. The threshold voltage concerning temperature is given below:

$$\frac{dV_{th}}{dT} = \frac{d\phi_F}{dT}\left[\alpha\sqrt{\frac{q\varepsilon_{si}N_{eff}}{\phi_F C_{ox}^2}} + 2 + \frac{qD_{it}}{C_{ox}}\right] \quad (4)$$

Where Εsi and q are the silicon permittivity and electron charge respectively. Value of α is 1 for partially depleted devices and α=0 for fully depleted transistors. Not only does the Vth increases with decrease in temperature but also the region of operation of the transistors depend upon the same [10].

Effect on Mobility:

The mobility in a MOSFET is affected by three factors Coulomb scattering, phonon scattering and surface roughness scattering. Out of these the Coulomb scattering and the phonon scattering depends on temperature. And the relation between these is given by the relation [9],

$$\mu_{ph}\alpha T^{-x} and \mu_c \alpha T \quad (5)$$

Where, x=1;77K<T<100K x=1-1.5; 100K<T<450K

Table 1
Device sizes

Transistors	Device Models				
	130nm	90nm	65nm	45nm	32nm
M1	1/0.39	1.5/0.27	1/0.195	2/0.135	0.6/0.096
M2	1/0.39	1.5/0.27	1/0.195	2/0.135	0.6/0.096
M3	3/0.39	0.8/0.27	0.5/0.195	1/0.135	0.3/0.096
M4	3/0.39	0.8/0.27	0.5/0.195	1/0.135	0.3/0.096
M5	2/0.39	2/0.27	1.5/0.195	3/0.135	1/0.096
M6	6.5/0.39	2/0.27	1.5/0.195	3/0.135	1/0.096
M7	2/0.39	4.5/0.27	3.8/0.195	6.5/0.135	2/0.096
M8	2/0.39	1.5/0.27	1/0.195	2/0.135	0.5/0.096

Table 2
Comparison of performance

Technology Node	32nm	45nm	65nm	90nm	130nm
Supply Voltage (V)	0.9	0.9	0.9	0.9	1.3
Power Dissipation (μW)	5.52	8.51	8.08	17.02	25.23
Differential Gain (dB)	67.04	70.37	73.59	74.8	80
Load Cap (pF)	2	2	2	2	2
Iref (μA)	5	5	5	10	10
Slew Rate (V/μSec)	0.9566	0.763	1.2274	0.5764	0.8068

4. Conclusion

To verify whether the designed circuit can deliver the required performance, the circuits are simulated using the NgSpice simulation software and also with the Mentor Graphics simulation tool using the BSIM4 technology PTM files on NgSpice. The 130nm PTM file has a gate oxide length of 1.6nm for both NMOS and PMOS transistors. Sufficient supply voltage of 1.3V DC is selected to overcome the threshold voltage of 0.3782V for NMOS and -0.321V for PMOS transistor.

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