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Structure Design Engineering for Optimal Analog Performance of Nanowire Junctionless MOSFET

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***Abstract*: Analog performance of silicon nanowire junction less MOSFET (SNW-JL-MOSFET) in the sub-20 nm regime is investigated using a device simulator, namely ATLAS. It is observed that optimal selection of structure parameters of SNW-JL-MOSFET attains higher drain current, peak trans conductance and output conductance. This proposed architecture also provides better analog frequency parameters and switching speed of the device and is very useful for circuit design. The gate dielectric material optimization of the structure is attained through via broad device simulation. In this manuscript, a study is carried for the SCEs like SS, DIBL and significantly for analog parameters like trans conductance and output conductance.**

***Keywords*: Charged Plasma, Dielectric Constant, Tunnel Field Effect Transistor (TFET), Tripple Gate (TG), Neutral Biomolecule.**

1. Introduction

The Gate All Around (GAA) silicon nanowire Field Effect Transistor (FET) has appeared as a high performance device structure to down-scale the upcoming nanoscale semiconductor devices due to higher packaging density, best gate controllability, and good potential to withstand Short Channel Effects (SCEs) [1]-[4]. Although with all the advantages, GAA nanowire FET has a disadvantage of high series resistance ocurring as an abrupt junction develops between densely doped source/drain and minutely doped silicon body [5], [6]. The solution for such problem is the formation of Junctionless (JL) nanowire FET [7]. Due to carrier transport mechanism, the JLFET based devices are addressed as accumulation mode devices. However, the conventional FET based devices are simply named as inversion mode devices. The JFET is developed by heavly doping the source, drain and channel regions uniformily throughout [8]. The heavly doping of the channel, the JL-nanowire undergoes a problem such as lower drive current (as of reduced carrier mobility) [9] or reduced transconductance [7], [9], [10]. JL nanowire FET possesses higher sensitivity due to heavy doping towards random dopant fluctuations (RDFs) [11], [12]. A solution to these problems, as proposed by Ramond et.al. [13] is GAA charge plasma-based dopingless FET nanowire. On introducing an n/p-type of plasma in intrinsic-type silicon, the development of source and drain regions is made possible with usage of suitable work functions. This concept removes doping requirement and clears doping control issues, namely doping activation, doping fluctuation and sharp doping profile [14]. Charge plasma concept is further applied to bipolar transistors [15], tunnel FET (TFET) [16], [17] and MOSFET [18]-[20]. A charge-plasma device produces a reduced thermal budget and provides better drive current, sub-threshold slope, and on-off current ratio. It further provides a higher immunity towards variation in parameters due to RDF in comparison to its junctionless counterparts.

The construction of multiple gate FET (MGFET) and 3-dimensional structures like dual gate (DG), Omega/FinFET and GAA FETs reveals a superior over the planner devices with sharp CMOS-scaling. In addition, the GAA-MOSFET is regarded as the final candidate for downscaling of device less than 50 nm [4] that provides higher packing density, steeper sub-threshold slope and high current driving capability. The GAA-FET critically contracts the SCEs because silicon layer is fully covered by entirely gate and thus, it controls channel's electrostatic potential effectively [5–9]. However, an extremely scaled devices are critically poor due to higher series resistance which occurs by construction of immediate source or drain junctions [10,11]. The significant solutions like Schottky-Barrier source or drain or JL-MOSFETs are extensively proposed and investigated [12]. The JL-MOSFET shows highly doped source or drain or channel regimes in a uniform manner, thus showing no PN junction creation within the source or drain and channel. However, highly concentrated doping of channel decreases the carrier mobility, which affected the device drive current as well as transconductance of [13]–[15]. All these disadvantages made the doped source-drain regions to be replaced with Schottky Barrier metal source or drain that offers raised on-current as well as improvement transconductance to JL MOSFETs.

The lower work function of device gate regime related to drain side has considerably lowered the peak electric field and hot carrier effects. And, the fabrication viewpoint complicated and robustly amalgamated two separate work function of metals as gate electrode. As it depends upon a single reactive ion etching process to patterning the dissimilar gate metals together.

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The dual material gate technology has enhanced the device immunity over the SCEs [18]-[19]. The new engineering stretched to DG MOSFET further improved device performance [20]-[21]. The integration of the gates is made possible via flow of fully-silicided metal (FuSi) [22]-[23], wet etching process [24], inter diffusing metal [25]-[26], selectively patterning and implanting of gate work functions. A finely thick dielectric layer covering finely thin SiO_2 layer for constant EOT has significantly reduced the gate tunnelling current.

2. Proposed Device Structure

Fig. 1 depicts silicon nanowire junctionless MOSFET (SNW-JL-MOSFET) and the experimented ON current characteristic.

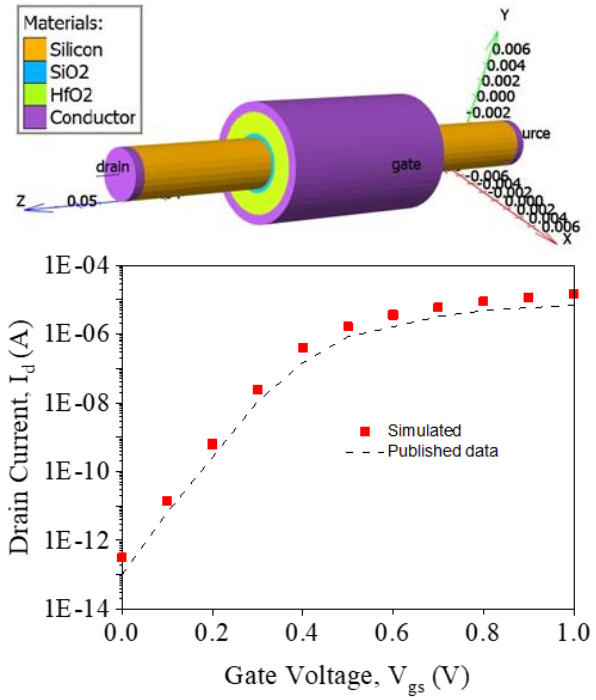

Fig. 1. Cross-sectional view of a) Conventional charge plasma TFET, b) CPB-TG-TFET biological sensor device c) Experimented characteristics of charge plasma based TFET structure simulated output current with conventional doping-less TFET

The device simulations are performed via ATLAS simulator [31] for performance computation of silicon nanowire junctionless MOSFET (SNW-JL-MOSFET), as shown in Fig. 1. All these architectures with gate length L = 20 nm, radius of Si film = 2.5 nm and oxide thickness tox1 = 0.4 nm (SiO2) and tox2 = 2.1 nm (HfO2) with high-k gate dielectric are acquired by setting work-function of the metal gate to have the same I_{off} with drain bias of 1.0 V. A high amount of doping of source/drain and channel regions with n-doping concentration (N+) of 1×10^{19} cm^{-3}. The geometrical limitations used for simulation of proposed device (NW-JL-MOSFET) are determined in Table 1.

The mobility models modulated for simulation are concentration dependent based on mobility as well as high-field reduction model [26]. Recombination model used here is Auger. The Shockley-Read-Hall generation/recombination model as well as band gap narrowing [19] are also employed. To account for quantum confinement effect, Bohm quantum model (BQP) is also included [18].

Table 1
Device Value of CPB-TG-TFET

Parameters	Values
Gate Length, (L nm)	*20 nm*
Source Length (L_S nm)	*10 nm*
Drain Length (L_D nm)	*10 nm*
Gate oxide, (t_{ox} nm)	*HfO_2 (2.1 nm) + SiO_2 (0.4nm)*
Silicon film doping, N_+ (cm^{-3})	*$1x10^{19}$*
Gate/Metal work function (eV)	*3.9 eV*

Calibration characteristic: The stimulated outcome of conventional dopingless TFET with the marked work in [13] is depicted in Figure 1(c). Tue reported data has been found via Plot Digitizer tool.

3. Results and Discussions

Junctionless transistors are basically the variable resistors controlled via a gate electrode. The channel made using silicon nanowire is heavily doped which can be fully depleted to switch the device into off state. The electrical characteristics of the device are similar to normal MOSFETs, however the concept is quite distinguished. The conduction mechanisms in Junctionless Nanowire Transistors (gated resistors) in contrast to inversion-mode and accumulation-mode.

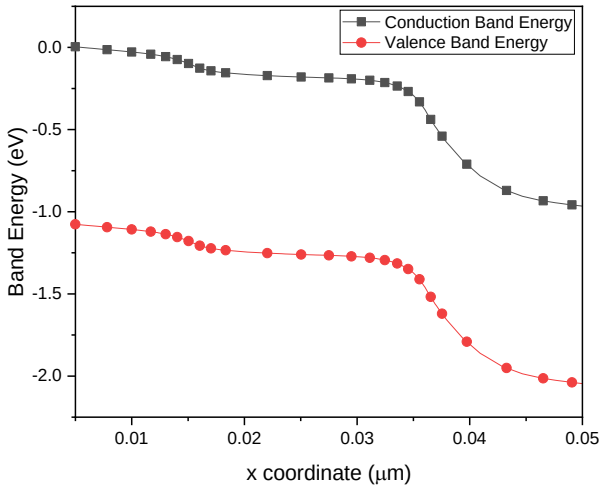

Fig. 2. Energy band diagram of a SNW-JL-MOSFET when $V_{gs} = V_{ds} = 1V$

MOS devices as represented in Fig. 2a shows the energy band diagram of SNW-JL-MOSFET for ON state (V_{gs}=1 V, V_{ds}=0V). As shown in Fig. 2a, the device with substrate doping $1x10^{19}$ has an energy barrier width within intrinsic channel and the partially depleted n-layer. In case the n-layer insertion is very highly doped with a high concentration, it hinders the electric field of source from exerting into the channel region. Thus, a significant quantity of electrons are shifted within drain, which indicates n-p insertion layer with fully doped probably act as an electron source instead of energy barrier. The effect is more pronounced when only a negligibly few electrons are expected at V_{gs}=0V in comparison to electrons from n-p layer

is negligibly a part of current conduction with V_{gs}=1 V.

Fig. 3 depicts the I_d-V_{gs} transfer characteristics of silicon nanowire junctionless mosfet (SNW-JL-MOSFET) at two different drain to source voltage (Vds= 50 mV and 1V) when gate to source voltage varying from 0 to 1 V. One can see from Fig. 3, the leakage current (I_{off}) is varying in between 10^{-15} A and 10^{-17} for two different drain voltage. Fig. 4 depicts that I_d-V_{gs} transfer characteristics of silicon nanowire junctionless mosfet (SNW-JL-MOSFET) at three different gate to source voltage (Vds= 0.8V, 0.9V and 1V) when drain to source voltage from 0 to 1 V.

However, from Fig. 3 and 4, it is found that with rise in dielectric permittivity over single oxide layer, the I_{on} and leakage current rises w.r.t fringing field effect. In case of high-k at interfacial oxide (SiO_2) layer, a reduction is found in device gate leakage current. The gate capacitive coupling increases which causes the leakage current to reduce [16]. The standby power of CMOS is effected by the sub-threshold or leakage current. The drain current of the junctionless nanowire is in direct proportion to nanowire cross-section and channel doping concentration but not for the gate oxide capacitance. Fig. 3 shows that I_{on} current at Vgs = Vds = 1 V in junctionless nanowire transistor with Lg = 20nm, is a function of device width and doping concentration.

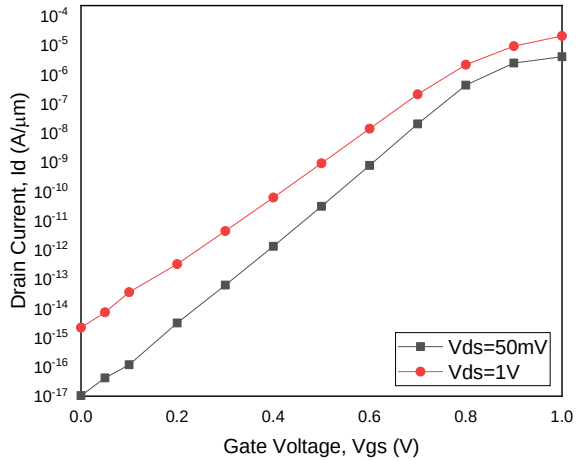

Fig. 3. Drain current (Id) vs. gate-source voltage (V_{gs}) for two different drain voltage i.e. V_{ds} = 50 mV and V_{ds} = 1V

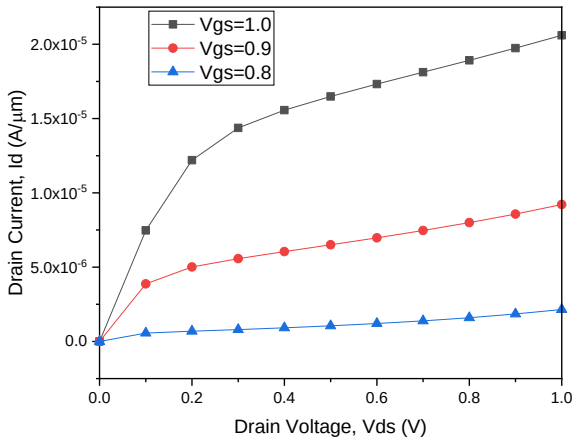

Fig. 4. Drain current (Id) versus drain-source voltage (V_{gs}) for two different drain voltage i.e. V_{ds} = 50 mV and V_{ds} = 1 V

A. Analog Performance

The crucial parameters including trans-conductance (gm), and output conductance (gd) are analyzed and discussed here from viewpoint of analog circuit analysis.

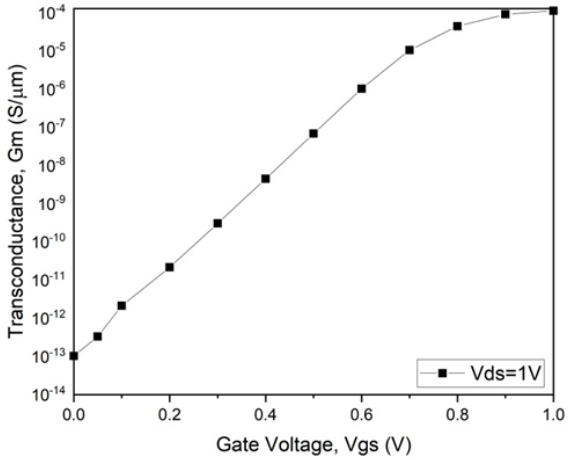

Fig. 5. Transconductance (gm) vs. gate to source voltage for V_{ds}= 1V

In Fig. 5, the transconductance (gm) Vs. gate-to-source voltage at V_{ds} = 1V is presented. The gm of MOSFET which determined amplifier gain as shown in Eq. (1). An improvement in gm, gives the higher carrier transport efficiency for the given gate stack configurations is essential for the analog applications.

$$g_m = \partial I_d / \partial V_{gs} \quad (1)$$

For computing output conductance gd, formula in Eq. (2) is utilized.

$$g_d = \partial I_d / \partial V_{ds} \quad (2)$$

The drain current rises with increase in dielectric permittivity over single layer configurations which eventually causes higher gd high for such configurations. The analog circuits, especially CMOS needs low output conductance (gd) transistors to receive high gain. High gd means, low output resistance which results in higher I_D with V_{DS} in saturation domain. The device components are associated with this increase, namely channel length modulation (CLM) and DIBL. On the other hand, an increase in the gate length of proposed device decreases the gm and consequently reduces the gm/gds.

4. Conclusion

This paper describes the conduction mechanisms in transistors based on junctionless nanowire. These devices do not function properly in inversion mode or accumulation mode, exceptionally in full/partial depletion. The threshold voltage depends on nanowire doping, EOT, width and thickness. In addition, the concept of a bulk multi-gate MOSFET is proposed without any lateral source/drain junction. Its demonstrated that JNT for shorter gate lengths can show low leakage currents and short channel behavior at shorter gate lengths. The gate dielectric material optimization of the device is achieved

through via extensive device simulation. In paper, a study is carried for the SCEs like SS, DIBL and significantly for analog parameter (FOMs) like transconductance and output conductance. It is found that single oxide layer gate dielectric devices with gate stack is improved the device performance and analog performances of the proposed device. So the proposed nanoscale silicon nanowire junctionless MOSFET may be considered as a suitable candidate for the design of Analog and RF circuits.

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