International Journal of Research in Engineering, Science and Management
Volume 4, Issue 9, September 2021
https://www.ijresm.com | ISSN (Online): 2581-5792

Application of Isolation and Protection Circuit for IGBT Gate Driver

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***Abstract*: Objective of this paper is to discuss the state of art IGBT Gate driver design, which includes the different isolation techniques, compatibility with power device and advanced protections feature. As the industry pushes for higher power and higher switching frequencies power supplies, which use IGBTs for power conversion. Reference to this, IGBT gate drivers is being designed to their ultimate attainable efficiency, smallest footprint, size and weight. Design and development of the Gate driver relates to the expertise on the circuit design and power devices operating characteristics. The subject is vital in order to adopt the modern design for critical operation (i.e., Traction, Healthcare, Energy).**

***Keywords*: Control signal, FWD, IGBT, Diode, Gate-driver, Isolation.**

1. Introduction

The Insulated Gate Bipolar transistor (IGBT) combines the MOSFET (metal oxide semiconductor field effect transistor) and BJT (bipolar junction transistor). IGBT has the fast-switching capability of the MOSFET (voltage controlled) and is capable of handling the high current values typical of a BJT. In addition, IGBTs have a lower on-state voltage drop and are capable of blocking higher voltages. For designing the gate driver device dynamic & static switching characteristic, safe operating area, topology implemented, and load characteristics shall be considered.

Static characteristics of the IGBT relates to the collector current I_C, Gate emitter voltage V_{GE}, Collector emitter voltage V_{CE} and Junction temperature T_J. For designing of gate driver static characteristics of the IGBT shall be considered from the datasheet of IGBT. V_{CE} defines a collector-emitter voltage drop in the ON state, and is used to calculate the power loss of the IGBT. Smaller the V_{CE} value, lower is the power loss. V_{CE} increases with increase in collector current I_C and V_{CE} decrease with V_{GE} value.

At lower collector current I_C, T_j increases as V_{CE} decreases. For higher collector current I_C, T_j decreases when V_{CE} increases. So V_{GE} is most important factor for power loss. IGBT drivers decide the V_{GE} characteristics.

Dynamic characteristics includes the switching of the device. T_{on}, T_{off}, E_{on} and E_{off} are the switching parameters of the device.

Increase in the switching time causes more switching losses. Lower the switching time may lead the higher turn off voltage because of higher Ldi/dt.

For inverter operation the dead time is to be seen with the T_{off} of the switching device. Higher T_{off} and unappropriated dead time may lead the short circuit of the upper and lower IGBTs of the same leg.

Optimum power supply capacity of the gate driver is defined by the gate charge capacity of the IGBT. Gate charge capacity is derived by the capacitance of the IGBT junction.

Dynamics characteristics of the IGBT shall be checked with the SOA (Safe operating area) for both the region (forward and reverse) and in reference to short circuit safe operating area (SCSOA). Selection of the gate driver hardware is to be seen in reference to the EMI-EMC compatibility.

The reverse-recovery time and turn-on time of FWD can be controlled by adjusting the switching of the IGBT. Losses in the device (IGBT and FWD) can be reduced by selecting the appropriate value of dV/dt. Other way of reducing the FWD losses in a bridge configuration is to turn on the IGBT with a reduced V_{GE}. This limits the peak reverse recovery current I_{rr}, of the FWD in the opposite side of the arm.

Static, dynamics, and operational conditions of the IGBT discussed as above is defined by the Gate driver i.e., V_{GE}, R_{gon} and R_{goff}. Vital role of the IGBT gate driver has to be evaluated in all aspects. Implementation of gate driver with above consideration is realized in laboratory, consideration of protection and insulation adopted and summarized.

2. Gate Driver Circuit Realization

A. Requirement of the Gate Driver

Gate drivers is intelligent hardware, offers reliable interfacing between control and power voltage level.

The primary function of the gate drive circuit is to convert logic level control signals into the appropriate voltage and current for efficient and reliable switching of the IGBT module.

An output stage of driver circuit consisting of small power MOSFETs, or bipolar transistors performs the conversion by alternatively connecting the IGBT's gate to the appropriate on (V_{on}) and off (V_{off}) voltages. Gate driver circuits also provide isolation so that the logic signals are not connected to the dangerous high voltage present in the power circuit. The driver must also be immune to the severe electromagnetic noise produced by the fast switching, high voltage, and high current IGBT power circuit.

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1) Turn on and turn off logic level

In reference to the collector-emitter conduction in an IGBT module a positive voltage must be applied to the gate with emitter. Maximum gate emitter voltage is specified on the device data sheet. V_{GE} greater than the specified value may cause breakdown of the gate oxide resulting in permanent damage to the IGBT. V_{GE} upper limit is linked to the short circuit time survival of the device. Most of the IGBTs are subjected to a low impedance short circuit for 10µs with suitable V_{GE}. V_{GE} lower limit is defined by the gain and switching losses of the device. Lower V_{GE} may be enough to turn on the device but for efficient switching it has to be selected properly. Static, dynamic and operational characteristic of the device is influenced by V_{GE}.

Device datasheet includes the turn off bias voltage. Turn off bias voltage offers the lower turnoff loss and also provide the dv/dt noise immunity. For Hi-voltage IGBT, effective $-V_{GE}$ turn off voltage shall be considered to avoid the noise immunity. Hi-Power IGBTs multiple chips is connected in parallel. This requires effective $-V_{GE}$ turn off voltage for insurance of avoiding the spurious switching built due to the IGBT junction capacitance and gate resistance of parallel chips.

2) Gate driver power estimation and peak current

Gate Driver Average current is decided by the switching frequency f_{sw} and the gate charge Q_g of the device.

Average drive current $I_g = f_{sw}*Q_g$.

From transition of V_{GE}, total gate charge can be estimated and switching information is already known to the designer.

Power of the gate driver can be estimated by the transition of the switching voltage $V_{GE\,(tr)}$.

Gate driver power, $P_g = f_{sw}*Q_g*V_{GE\,(tr)}$

The peak gate current is decided by the gate resistance and transition of the switching voltage $V_{GE\,(tr)}$.

$I_{gp} = V_{GE\,(tr)}/R_g$.

Gate driver power and the peak current calculation is the basic requirement for designing the gate driver.

3. Gate Driver Power Supply

IGBT Gate driver need its own isolated power supply. The base board of the gate driver circuit has the power supply circuit. Modern state of the art gate driver core has the isolated power supply included in it along with the control signal isolation pulse transformer.

The critical requirement of the power supply is V_{on} and V_{off} as according to the switching characteristics, requirement of floating power supply arises because of emitter potential of IGBT driven in most of the topologies.

The Power supply shall not have any current limitation for short time current requirement. Output behavior of the power supply shall not have any limitation with respect to overloading and hiccups. The rising of output voltage shall be continuous & uniform and the output characteristics shall be noise immune. The gate drive power supply should provide voltage insulation for reliable operation. Power supply shall have minimum capacitance in section to avoid the noise generated from dv/dt.

4. Gate Driver Control Signal isolation

Isolation is the other requirement which has to be considered for the selection of gate driver concept. Device rating or maximum voltage seen by the semiconductor defines the isolation requirement. Optocouplers, Fiber optical, pulse transformers are used for insulation between gate driver control and power side.

1) Optocoupler isolation

For driving high power side in any topology, opto-couplers can be used with the advantage of very high isolation voltage. 2.5kV to 5kV isolation is achievable by use of properly certified opto-couplers. Signals from DC to several MHz can be handled by opto-couplers. Microcontroller/DSP/PWM IC can be interfaced to optocoupler easily.

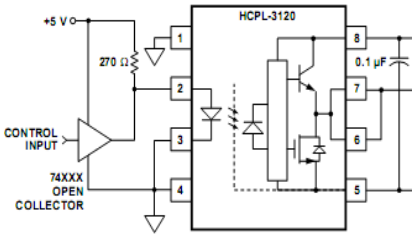

Fig. 1. Standard Optocoupler HCPL-3120 Optocoupler

Input resistance 270Ω of the circuit is designed according to the input current and voltage drop of the diode given in the reference datasheet. One disadvantage is that the opto-coupler adds its own propagation delay. Another disadvantage of using an opto-coupler is that separate isolated power supply is required to feed the output side of the opto-coupler and the driver connected to it. However, isolated DC-to-DC Converters with few thousand Volts of isolation are readily available. These can be used to supply isolated and regulated +ve 15 V and –ve 15V to the output side of the opto-coupler.

2) Fiber optical isolation

Fiber optical isolation techniques is widely used for the high-power traction application which offers higher level of isolation. Fiber optical transmitter and receiver is designed as per reference datasheet.

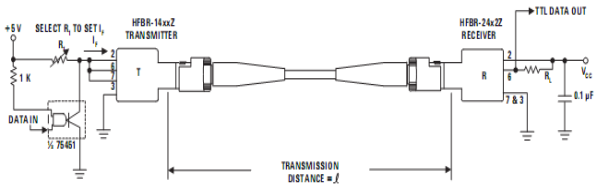

Fig. 2. Fiber optical transceiver

From datasheet, the maximum forward input current of QFBR 1478 (Transmitter) is 15mA. Now with an input pulse voltage of 15V the input resistance should be,

$$R_{35} = \frac{V_{CC} - V_F}{I_F}$$

$$R_{35} = \frac{5 - 1.2}{15mA}$$

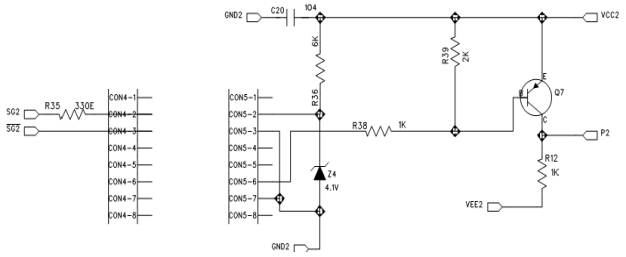

Fig. 3. Transmitter and receiver circuit design

$$R_{35} = 230 \text{ ohms}$$

Design of R_{36} *:* From datasheet the maximum output current of QFBR 2478 (Receiver) is 200mA.

$$R_{38} + R_{39} = \frac{V_{CC}}{I_O}$$

$$R_{38} + R_{39} = \frac{18}{200mA}$$

$$R_{38} + R_{39} = \frac{18}{200mA}$$

$$R_{38} + R_{39} = 100\ ohm$$

$$R_{38} + R_{39} = 3\ kohm$$

3) Isolation by pulse transformer

Using pulse transformers to achieve galvanic isolation is a frequently used technique. Depending on the range of frequencies being handled and power rating (voltage and current ratings and ratios), transformers can be designed to be quite efficient. The gate drive transformer carries very small average power but delivers high peak currents at turn-on and turn-off of the power device.

While designing or choosing a Gate Drive transformer, the following points should be kept in mind: Average power being handled by the transformer, margin of safety, required maximum volt-second product value and allowing for worst-case transients with maximum duty ratio and maximum possible input voltage. Employing bifilar winding techniques to eliminate any net DC current in any winding. This is to avoid saturation.

If operation in any one quadrant of B-H loop is chosen, care should be taken for resetting the core. Advantages of employing transformers for Gate Drive is that there is no need for any isolated DC-to-DC Converter for driving an upper MOSFET/IGBT. There is practically no propagation delay in a transformer to carry signals from primary side to the secondary side. Several thousand volts of isolation can be built in between windings by proper design and layouts. Fault at secondary side and feedback mechanism is also managed with the dedicated pulse transformer. The disadvantages of using pulse transformers for Gate Driver is that pulse transformer can be only used for time varying signals.

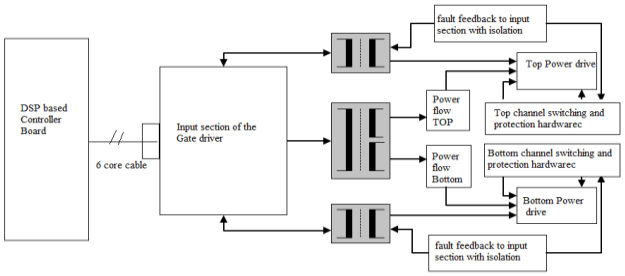

Fig. 4. Transformer core for isolation and feedback

5. Gate Driver Hi-volt section

Gate driver Hi-volt section connect with the power device, it includes the signal/fault processing, protections and switching control hardware.

1) Short circuit protection

$V_{CE\ sat}$ is the optimum solution for the short circuit protection. IGBT datasheet provide the information to survive low impedance short circuits, generally a minimum of 10µs. Typically, this short circuit protection is provided by collector emitter voltage sensing or so called "desaturation detection".

The circuit of $V_{CE\ sat}$ is realized in Fig 5. High voltage fast recovery diode D_1 is connected to the IGBT's collector C_1, this is used to monitor V_{CE}. During the off state of device, Diode connected with collector is reverse biased and the input of the comparator is pulled up to $+V_{CC}$. When the IGBT turns on, the comparators input will see the $V_{CE\ sat.}$ In case of IGBT short circuit, the current will create the collector-emitter voltage above the defined $V_{CE\ sat.}$ This occurrence is called the desaturation. Desaturation condition can be linked logically linked with input on-state to firm the short circuit detection.

Delay in the $V_{CE\ sat}$ monitoring is realized by the RC network at the input of the comparator.

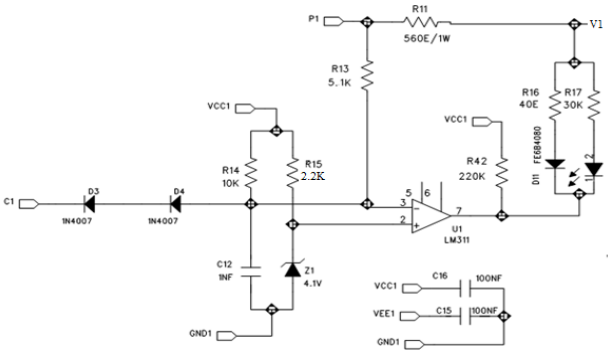

Fig. 5. Protection circuit

The delay should be such that it should be sufficient for the response of LM311 comparator and should not be more than the short circuit capability of the switch.

$$R_{14} * C_{12} = 10us$$

R14 is taken as 10k and C14 automatically becomes 1nF.

Desaturation and short circuit protection can be evaluated as per the test circuit below. Trip V_{CE} / $V_{CE\ sat}$ can be verified by shifting the diode and protection can be checked.

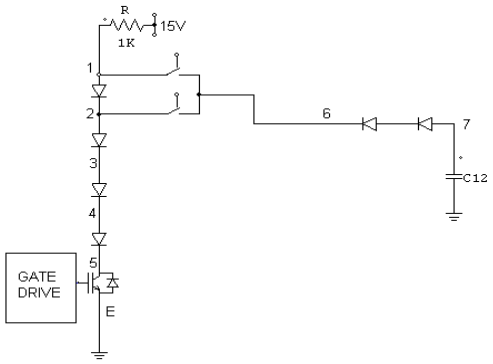

Fig. 6. Test circuit for V_{CE} monitoring

2) Gate resistance design

Gate resistance has a major role on the IGBT's switching characteristics. Lower value of the gate resistor offers fast charge and discharge of the gate capacitance which results in higher switching speed, lower switching losses and dv/dt immunity. Turn on gate resistance is limited by the driver peak current and freewheeling diode reverse characteristics. Higher value of the gate resistance reduces the turnoff transient but increases the switching losses. So, the optimum value of the gate resistance shall be checked including above parameters.

3) Interfacing of driver to IGBT module

Wiring between power module and gate driver shall be short to avoid the gate signal oscillation and noise. Twist wiring is preferred for the gate driver interface. Layout of cable should be EMI proof. Other phase gate driver interface cable shall be separated. In case of doubt on the gate cable implementation of gate emitter pull down resistor near the IGBT module is must for insurance of turn off the IGBT.

Gate over voltage protection can be built by connecting the Zener diode in between gate and emitter.

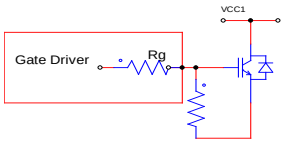

Fig. 7. Gate wiring open protection

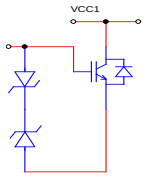

Fig. 8. Gate over voltage protection

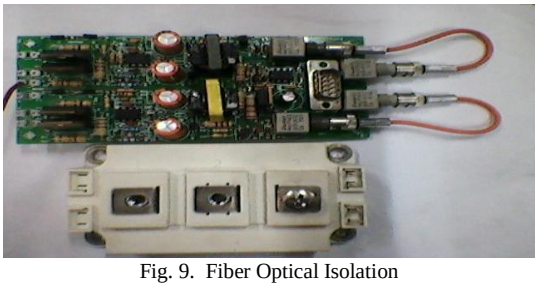

Fig. 9. Fiber Optical Isolation

Fig. 10. Optocoupler Isolation

Fig. 11. Pulse transformer Isolation

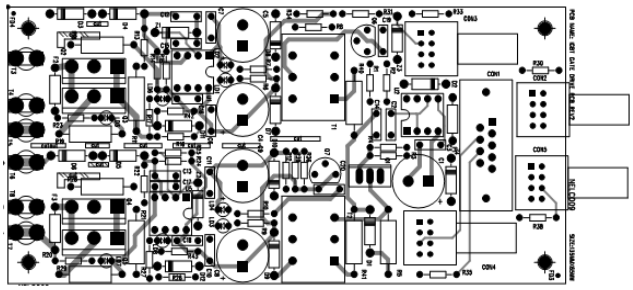

Fig. 12. Implementation of isolation techniques for gate driver

6. Conclusion

This paper includes the concepts of gate driver circuit design and realization which plays a critical role in power conversion. Gate driver interfacing, isolation techniques and consideration of static and dynamic characteristics of the device and protection circuits has been considered in designing of the gate driver circuit.

The paper gives the basic considerations and technical requirements for the gate driver design and optimization.

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