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Design of Low Power Comparator in 90nm Technology for ADC Application

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***Abstract*: Comparators are the most underrated and under-utilized monolithic linear component. In today's generation power dissipation is the most criteria in affecting the circuit we need to reduce the power dissipation. Choosing the best comparator for application is necessary. Here dynamic comparator has been designed and obtained a power dissipation of 78.14uW which is less than the power dissipation of pre-amplifier-based comparator. Design of low power comparator in 90nm technology for ADC application is done using cadence tool.**

***Keywords*: Power dissipation, ADC, Dynamic comparator, Technology, Pre-Amplifier comparator.**

1. Introduction

In today's modern electronics system ADC has become a key component. All the signals in the universe is measured using the analog, which has infinite set of occurrences. In order to overcome this, a digital component is designed which finite has set of occurrences. One of the component in ADC namely comparator compares the two voltages and gives a digital output. In particular type of ADC comparator is the major component leads to the more power dissipation of overall circuit.ADC requires less power dissipation, less delay, and high speed with reduction in offset. Low power consumption and high speed has been seen in ADC. Previously preamplifier-based comparator has been used but there is more power dissipation so here a dynamic comparator has been bought with low power dissipation compared to the preamplifier-based comparator.

2. Literature Review

In 2015, a high speed, ultra-low power designed using dynamic comparator for the applications of bio-implantable circuits and ADCs [3]. In this, presents the low power two stage dynamic latch comparator and that works in high speed and less power consumption. The proposed comparator as two stages they are, dynamic latch and preamplifier stage [4]. In this, the proposed comparator as several circuit level techniques for the performance of power dissipation and delay has done and the power preserving can be performed by leakage of transistors in the circuitry, and this point with regards to firm and low power dynamic CMOS comparator in 180nm technology [5], [6].This performance has different applications, but all of them craves some refine technology to support and change. The indicated techniques can be very useful for computer architects, where as in deciding the power apportion for the various units in the existence of leakage remission techniques [7]. In view of this, the work assesses the impact of process deviations on the electrical nature of a set of conjunctional cells as different transistors sizing methods: minimum sizing, logical effort and, delay-optimized sizing. The finest case fluctuation of robustness is accomplished by accepting the delay-optimized sizing technique [8]. In the midst of all the comparator designed, Double-tail comparator with shortened leakage has a less delay and low power. In the equal year power productive flash ADC can be accomplished based on a comparator composed using territory wall motion in a magnetic strip and MTJ [9]. The proposed that altered GDI contributes comfortable reduction of both sub-threshold and gate leakage current in comparison to static CMOS process in 45nmtechnology for 2-bit magnitude comparator and accordingly the drawback of GDI technique go through from fabrication intricacy in standard CMOS process. Thus, substrate terminal of PMOS and NMOS are connected to VDD and ground. The area consuming by the chip is reduced by modifying only 20 transistors [11]. The proposed comparator is the preamplifier-based comparator bearing more power dissipation [12]. To conquer this disadvantage, in this paper we have designed the circuit in such a way that the power dissipation and also the delay is reduced.

3. Operation of Comparator

Comparator compares two analog input and gives a single digital output. Let us consider V_p and V_n are the two analog inputs V_{out} is the digital output. V_{DD} is the dc voltage.

From fig. 1, if V_p is at a greater potential than V_p, then the output V_o of the comparator is logic 1 and when V_p is at a potential less than V_n, then the output is at logic 0. Fig. 2 shows the voltage transfer characteristic of ideal comparator.

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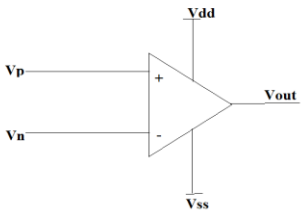

Fig. 1. Schematic of comparator

$V_p > V_n$, $V_{out}=1$
$V_p < V_n$, $V_{out}=0$

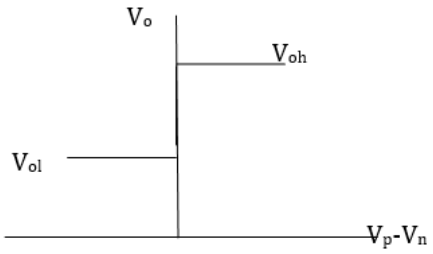

Fig. 2. Voltage transfer characteristic of ideal comparator

Some of the Comparators used are op-amp, single tail comparator and regenerative comparator. Op-amp acts as comparator without using the feedback. Regenerative uses a positive feedback to act as comparator. A single tail comparator has a transistor tail attached to its circuit with clock input.

A. Pre-amplifier based CMOS Comparator

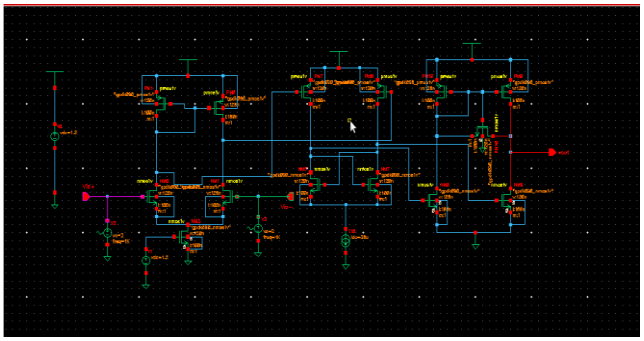

Fig. 3. Schematic diagram of pre-amplifier-based CMOS Comparator

Operation of CMOS comparator undergo three modes of operation namely preamplifier, latch, and buffer stage. From fig 3, preamplifier amplifies the weak signal which is an input to the amplifier; latch circuit gives a larger input signal and amplifies their difference. Analog to digital signal output is given by buffer circuit. The power dissipation in this comparator is relatively high due to its more number of transistor and area covered. Hence a very rarely used comparator in any application is CMOS comparator due to its disadvantages. Hence to reduce power dissipation a dynamic comparator came into existence.

B. Dynamic Latch Comparator

The disadvantage of CMOS comparator is that it has high power dissipation and delay compared to other comparators. In order to overcome this disadvantage so we design a dynamic comparator which gives low power dissipation, delay compared to above one. Figure 4 shows the schematic diagram of dynamic latch comparator.

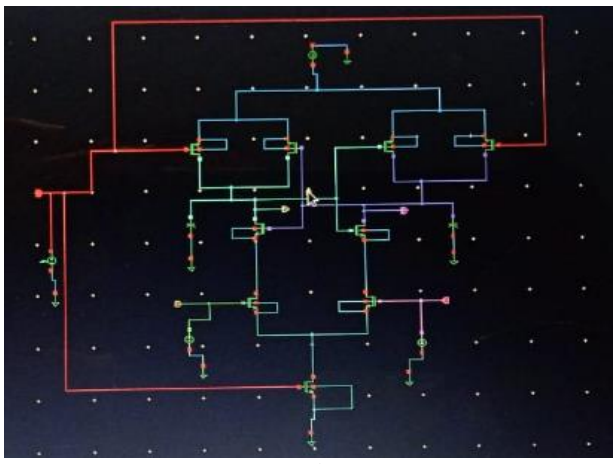

Fig. 4. Schematic diagram of dynamic latch comparator

Working: It consists of 9 transistors, 3 inputs and 2 outputs out of which M3, M4, M5, M6 acts as linear region, M7, M8 act as saturation region, M1, M2 act as saturation region, Mtail act as linear region. Output node n act as input to the M5, M8, whereas node n act as input to M4, M7. Operation undergo in 2 phases namely,

RESET PHASE: clk=0, Mtail=OFF, M3, M6=ON output n & p are charged to VDD logic 1 appears at both the nodes. These nodes are independent of Vinn &Vinp.

COMPARISION PHASE: clk=1, Mtail=ON, M3, M6 =OFF. Vinn & Vinp are given different voltages comparator compares these to voltages depending upon greater and lesser action is performed by M1, M2 transistor and gives a respective output.

4. Methodology

A. Objective1: Design Using 90nm Technology

Comparator has been designed in 90nm technology in cadence tool. The design of comparator has been done by considering W/L ratios. W/L ratios have been found by using the equation of drain current of both saturation and as well as linear region. The obtained values as been implemented in dynamic comparator and schematic diagram has been obtained using cadence tool.

B. Objective 2: Analysis of Performance Parameter

Analysis of performance has been done after getting the output. Performance parameters like Transient analysis, DC analysis and Delay analysis. Fig. 5 shows the transient analysis and stop time was given as 2ms and obtained a waveform.

Transient analysis undergoes two conditions:

When $V_{inp} > V_{inn}$, output p discharges at a much faster rate than output n which is shown in fig. 6.

When $V_{inp} < V_{inn}$, output n discharges at a much faster rate than output p which is shown in fig. 7.

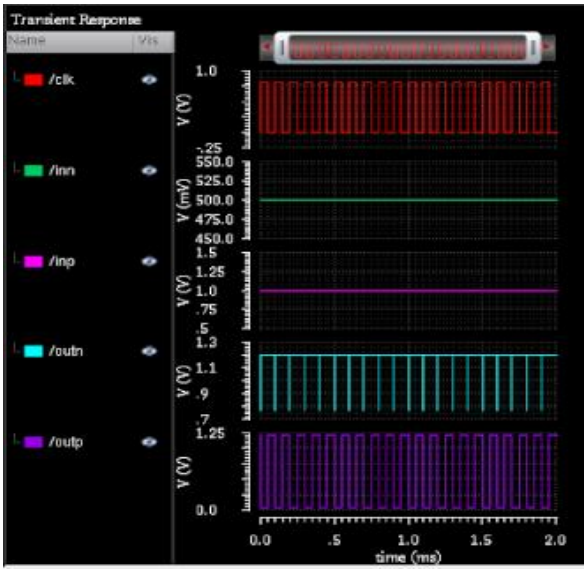

Fig. 5. Transient analysis of proposed Dynamic Latch Comparator

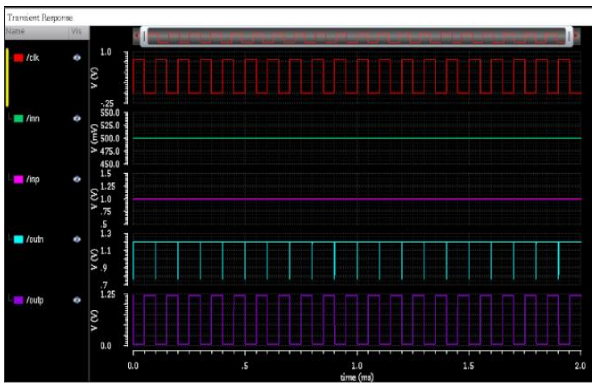

Fig. 6. Transient analysis (V_{inp}>V_{inn})

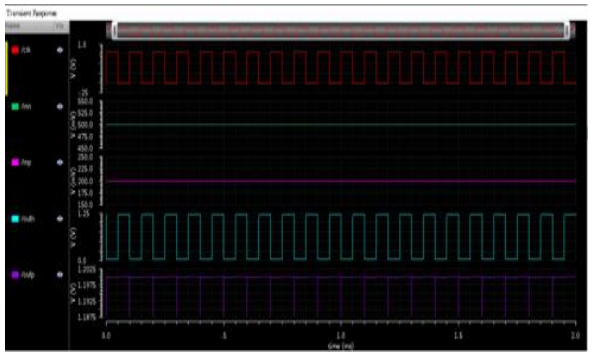

Fig. 7. Transient analysis (V_{inn}>V_{inp})

Delay analysis: Delay of dynamic latch comparator has been obtained by taking input as clk1 and output as outp. The obtained waveform is as shown in figure 6 with stop time 5 and threshold value as 0.6 v.

C. *Objective 3: Analysis of power dissipation*

Power dissipation is the process by which an electronic device produces heat as an undesirable derivation of its primary action. When power is dissipated, it invariably leads to rise in temperature of the chip. This rise in temperature affects the device both when the device is off as well as when the device is on.

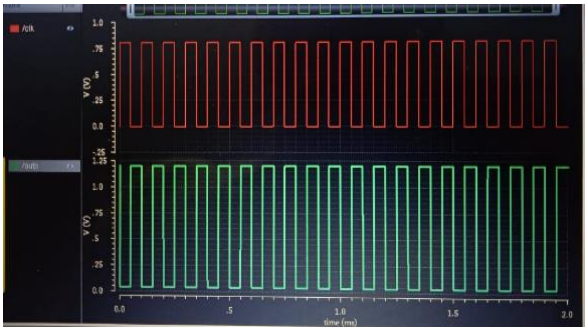

Fig. 8. Delay waveform of dynamic comparator

$$P_{dynamic} = \alpha C V_{DD}^2 f$$

Total Power = dynamic power dissipation + static power dissipation

DC analysis: Analysis has been obtained by giving stop time as -2 to 2 and obtained a waveform shown in fig. 9.

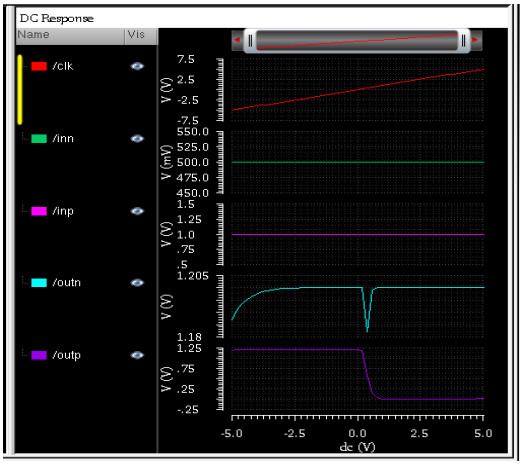

Fig. 9. DC analysis

Fig. 10 and 11 shows, total power of comparator and power of individual transistor is obtained in graph shown below.

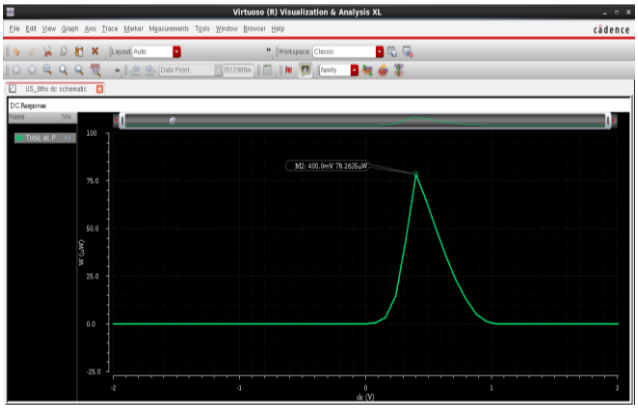

Fig. 10. Total power of comparator

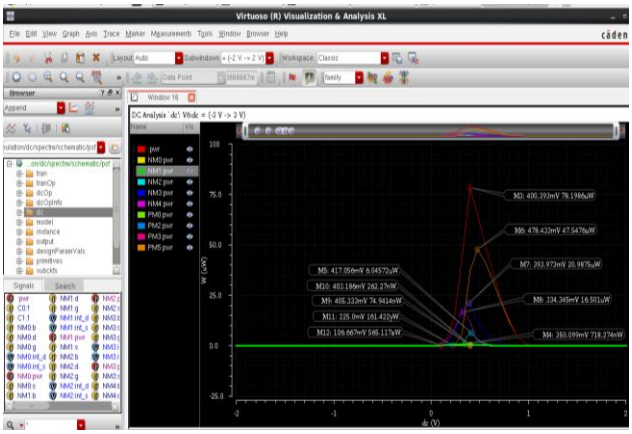

Fig. 11. Power of different transistor

D. Objective 4: Simulation using cadence tool

Cadence tool uses VLSI design which is full costumed and implemented. Design starts with MOS transistor and ends with direct schematic simulation. For transient analysis simulation is done using spice model files.

First design entry- MOS transistor design- library- GPDK 90nm.

1) Schematic capture of dynamic comparator

Schematic design of comparator has been done by selecting the required components in a browser of analog lib applied all the input and output ports and an input voltages consisting of PULLUP and PULL DOWN network. Even all the input voltages have been applied with respective value.

2) Simulation

Created a schematic and simulation is done with zero errors. Going on to Launch ADE L and setup has been given and selected transient and dc. Values were updated for a specification given to each parameter. In a schematic inputs and outputs were selected through output to be plotted and then applied for run. An expected output waveform was generated in a window. All the results have been calculated.

5. Result and Observation

From the above designed procedure, the result obtained is the Transient, DC, Delay and Power analysis for dynamic latch comparator Simulation of dynamic comparator is done with an expected waveform consisting of DC analysis and Transient analysis shown in fig. 12.

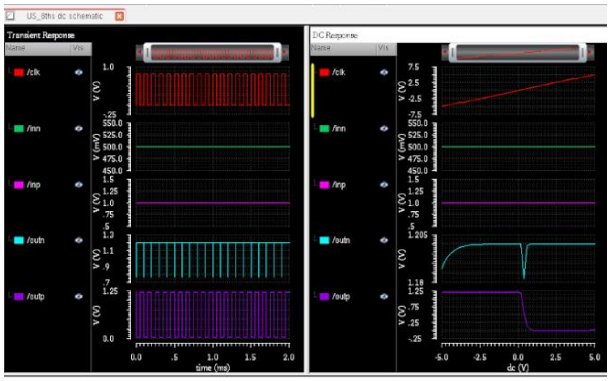

Fig. 12. Result of DC and Transient analysis

Observation has been made compared with the preamplifier-based CMOS comparator which is listed below in table 1.

Table 1
Comparison of pre-amplifier comparator and dynamic latch comparator

PARAMETER	PER-AMPLIFIER COMPARATOR	DYNAMIC LATCH COMPARATOR
TECHNOLOGY	90nm	90nm
NUMBER OF TRANSISTORS	14	9
DELAY	293.3u sec	50u sec
POWER DISSIPATION	360u W	78.14u W
FREQUENCY	100M Hz	10K Hz
SUPPLY VOLTAGE	1.2 v	0.8v
PERIOD	-	100m sec
RAISE TIME	2.727u sec	10p sec
FALL TIME	2.727u sec	10p sec
PULS WIDTH	-	50u sec

6. Conclusion and Future Scope

A low power dynamic comparator has been done for an ADC application in 90 nm technology using cadence tool by considering the parameters like delay power dissipation and delay and supply voltage with respect to preamplifier-based comparator. Power dissipation obtained is 78.14u W and delay obtained is 50u s. The future work can be done using 45nm technology and can be implemented in one of the applications.

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